

ARM has recently announced two new Cortex-R processors for high-performance, real-time applications such as mobile baseband. In this article we take a look at how these processors enable the next generation of mobile evolution as the cellular industry moves toward 4G fourth generation communications technology.

New Cortex™-R Processors for LTE and 4G Mobile Baseband

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Progress in mobile wireless communications continues unabated as subscribers consume new products and services using mobile devices with increasingly powerful feature sets and performance. By the end of 2010, more than four billion people worldwide were connected to mobile services using ARM-powered Low-Cost Handsets (LCH), feature phones, smartphones, tablet computers and USB modems for laptops. Explosive growth in the use of smartphones such as Apple’s iPhone, Google’s Android, RIM’s Blackberry and now Microsoft Windows Phone 7 devices has led to a total of 13 billion applications being downloaded to date with an astonishing 300,000 new Android devices being turned on every day! New generations of radio access technology for mobile communications have been developed to satisfy users’ increasing thirst for connectivity, data and interactivity.

The radio access technology used between mobile devices and base stations has evolved with the addition of data services on top of voice calls and messaging. Generations of wireless technology are the original analog 1G, the first digital generation called 2G, and today’s 3G, using clever modulation and data transmission schemes such as High-Speed Packet Access (HSPA) in newly allocated radio spectrum. Now the latest technology to be standardized is called Long-Term Evolution, or LTE, which will enable mobile technology to continue evolving through the 2010s and beyond. LTE will be the last 3G radio access technology and its successor, LTE-Advanced, will comply with the International Telecommunication Union’s requirements for a 4G system.

	WCDMA	HSPA HSDPA/HSUPA	HSPA+	LTE	LTE Advanced
Max DL rate	384 Kbps	14 Mbps	28 Mbps	100 Mbps	> 1 Gbps
Max UL rate	128 Kbps	5.7 Mbps	11 Mbps	50 Mbps	> 500 Mbps
Round trip latency	150 mS	100 mS	50 mS	10 mS	5 mS
3GPP release	Rel 99/4	Rel 5/6	Rel 7	Rel 8	Rel 10
Deployment	2003	2005 - 2007	2008	2009	~ 2014
Radio Access Technology	CDMA			OFDMA / SC-FDMA	
ITU Generation	3G	3.5G		3.9G	4G

Table 1: Mobile data standards

LTE will deliver voice, video and data at broadband data rates to mobile devices, enabling any-time, anywhere, always-on high-speed Internet access. Moreover, it will continue to provide service whilst users are on the move in a car or train, travelling at over 200 km an hour. A new generation of highly interactive multimedia mobile applications will be used on these new LTE devices. Imagine carrying a tablet computer out in the countryside anywhere in the world with instant access to maps, tour guides and low-latency interactive multimedia information relating to whatever you're standing in front of or viewing through the camera. However, LTE is an advanced technology and exceptionally large amounts of processing are required to support the high data rates required for new applications, particularly in the baseband where all the wireless signal processing takes place.

Powerful ARM Cortex-A processors enable mobile devices to run applications on a mobile software operating system together with other ARM processors performing auxiliary tasks for interfaces such as touch screens and connectivity such as WiFi, Bluetooth and NFC. However at the heart of every device there is also a baseband processor that is the digital system for transmitting and receiving data over the radio. In turn a baseband processor is divided in two parts – a modem to modulate and demodulate the radio signal and a protocol stack processor which manages the communication between base station and mobile terminal by establishing connections, managing radio resources, handling errors and packetizing incoming and outgoing data.

The tasks in the modem and protocol stack processing are distinctly different and can be thought of as operations in orthogonal planes with the protocol stack software being layered according to the OSI model as shown:

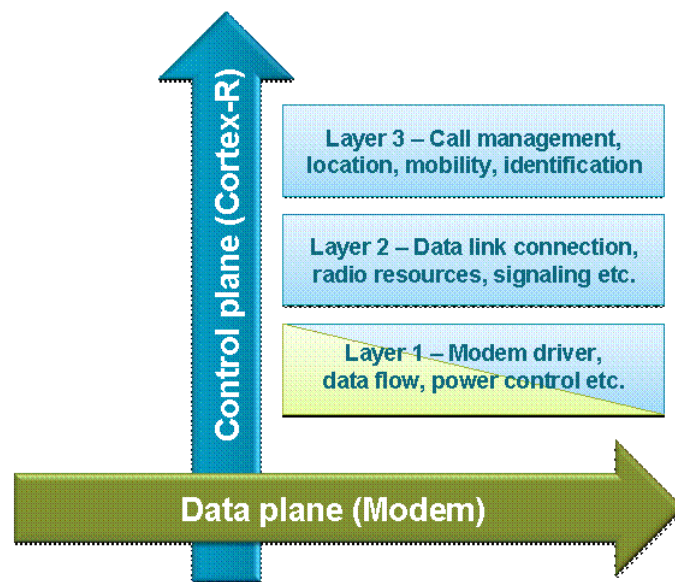


Figure1: Baseband processing planes

The data plane, or physical layer, is where digitized radio signals are processed in the modem; a system of very fast digital signal processing logic and localized hardware control blocks. This data plane processing is very intense as LTE received data is streamed out of the ADC at around 40 million samples per second with 12-bit resolution. Two streams of so-called I and Q radio data are presented and the streams are doubled or quadrupled for MIMO multiple antenna configurations. The modem's signal processing tasks are performed by

dedicated hardware incorporating specialized Digital Signal Processors (DSPs) with Very Long Instruction Words (VLIW) specifically designed for LTE's OFDM modulation technique.

The control plane is where layers-1, 2 and 3 protocol software stacks manage communications and present the software interface for voice, text and data communications, including video. The protocol stack software in the control plane can be many Megabytes of code and may also be required to support pre-existing 2G and 3G mobile wireless standards. Typically a Real-Time Operating System (RTOS) such as Nucleus or ThreadX will provide the control plane code environment.

High performance control software is also required at the lowest layer-1 to control the modem, manage radio resources, maintain connection with the base-station and respond to changing signal conditions, for example by dynamic adjustment of power levels and signal conditioning as the handset moves about. A very fast interrupt response is essential for maintaining reliable communications and these interrupts must be processed within the allotted time if LTE communications are to be maintained. Variations in modem architecture across different manufacturers can increase or decrease the layer-1 protocol stack task.

The protocol software stack for earlier 2G and current 3G radio access technologies often runs together with applications on a single general-purpose processor such as the ARM1176 which powers many of the mobile phones shipping today. These systems can allocate around a third of their processing to the baseband without compromising application performance. However, the latest generation of smartphones and tablet computers run far more demanding operating systems and multimedia applications with increasing features using HSPA or LTE. These increasing processing requirements and the complexities of chip design caused divergence between applications and baseband processing chips which have evolved into distinct semiconductor products in all but the very lowest cost handsets. This divergence is further emphasized by products such as data modem cards and 3G USB data modem sticks which contain only the baseband processor.

ARM Cortex-R processors are used for the protocol stack processing in these 'diverged' baseband processor chips for 3G HSPA and LTE, leading to 4G LTE-Advanced. These protocol stacks consist of a complex set of tasks that must meet demanding real time constraints if communication is to be maintained without data loss. The LTE and LTE-Advanced standards specify critical timings expressed in fractions of a millisecond which the mobile device must meet if it is to operate correctly.

Cortex-R real-time processors offer the requisite high performance, deterministic response time and excellent energy efficiency that is required for 3.9G/LTE and 4G/LTE-Advanced baseband tasks. The Cortex-R4 processor is already firmly established for this purpose and in January 2011 ARM announced two new real-time processors; Cortex-R5 and Cortex-R7. Examining the requirements for LTE and LTE-Advanced shows how these new processors are capable of meeting the levels of performance necessary to move beyond category-3 data rates whilst maintaining robust connections at cell edges with high mobility and acceptable energy efficiency.

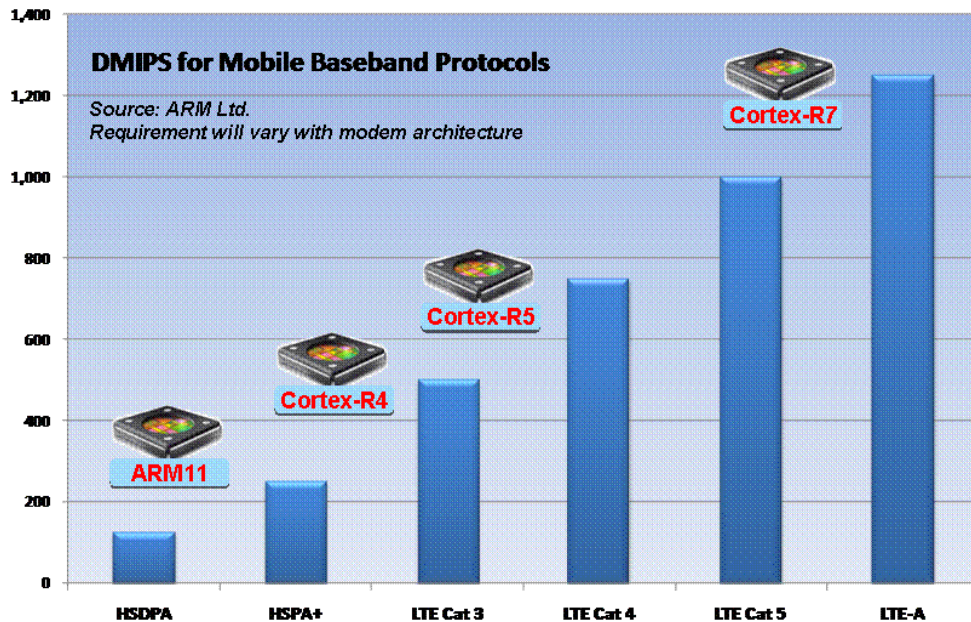


Figure 2: Baseband processing performance requirement

The performance required for baseband protocol stack processing depends on the architectural choices made in the modem design and associated hardware ‘accelerators’ for error correction, compression and encryption (ciphering). A Direct Memory Access (DMA) controller can offload the processor with specific features for managing fragments of data that are scattered and gathered in memory. Flexibility is also important in a modem design as dedicated hardware can result in products unable to adapt to changing requirements from network operators and international standards. At present, the complexity of LTE technology and differences in local implementations is driving a trend towards programmability as opposed to hard-wired logic solutions.

An LTE-capable mobile handset will probably have the generic system architecture illustrated here.

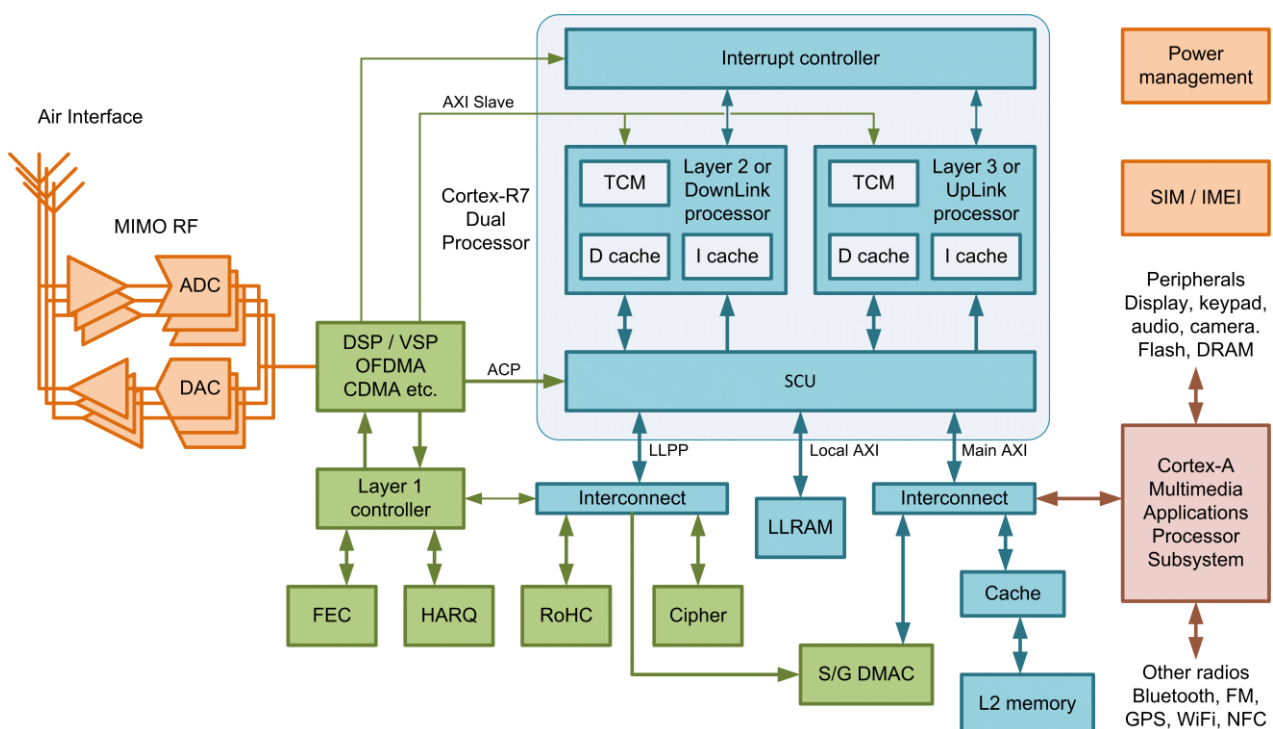


Figure 3: Illustrative baseband architecture

On the left is the radio comprising the antenna, transmit power amplifier, receiver, frequency up/down conversion and analog to digital conversion. Data sent over the radio is fed into or out of the modem, shown in green. The modem is responsible for coding and decoding the radio information to and from a data bit stream which is read in or out of baseband level-2 memory. The latest multi-standard modems occupy many millions of gates in silicon and their designs vary widely across different baseband chip manufacturers where some have evolved over many generations of mobile technology. Chip manufacturers use different architectures that differentiate their capabilities and performance, although the same hardware and/or software architecture is often adapted for different purposes, e.g. LCH, feature phone, smartphone or data card. An associated applications processor is shown in red on the right. This could be connected via USB.

Incoming and outgoing data is managed by a dual core protocol stack processor, shown in blue. System designers will probably opt to run layer-2 code on one processor and layer-3 on the other, taking account of interrupt distribution. Interrupt performance is key because modem hardware typically generates around 50 interrupts that must be promptly serviced and designers will probably want to route a small number of critical high frequency interrupts to one processor whilst the other supports more periodic events with larger service routines. Some layer-1 control exists in modem hardware but it may also require support from the layer-2 processor.

High performance processors with a fast and deterministic interrupt response are required to run these software stacks. Approaches to system design vary, but quite often a separate processor is preferred for each layer and this can relax clock frequency and energy consumption, simplify memory implementation and partition the software for simplicity and performance benefits. A dual processor system like this will generally provide the most energy-efficient architecture for longer battery life and reduced heat dissipation. A deterministic interrupt response is critical in this application – if the processor is otherwise busy and does not guarantee to service interrupts on time, every time, then data can be lost and the connection can drop!

This class of baseband processing application is precisely what the ARM Cortex-R real-time processors are intended for. The new Cortex-R5 and R7 processors are described in detail elsewhere in this issue but some features are particularly relevant to this baseband architecture as follows:

High Performance: Cortex-R5 and R7 cores provide 1.66 and 2.53 DMIPS/MHz respectively, which should meet the most demanding baseband processing requirement.

Coherency: Cortex-R5 and R7 contain a Snoop Control Unit(SCU) which automatically maintains coherency between modem data fed into memory and the processors' data cache. This can save considerable software overhead. In the case of Cortex-R7 there is also provision for coherency between the two processors.

Low-Latency Peripheral Port (LLPP): An additional AXI bus port specifically purposed for fast control of modem hardware without being blocked by large data transactions on the main AXI bus.

Low-Latency RAM (LLRAM): An area of memory used to hold critical software and data such as Interrupt Service Routines (ISR) that can be executed almost immediately without waiting for main AXI bus transactions to finish and/or for the ISR to be fetched into level-1 cache.

Tightly-Coupled Memory (TCM): A limited (128 KB) memory resource for the most critical code and data that can be accessed without the latency incurred by an AXI bus port. This provides for the highest level of deterministic response to real-time hardware such as an LTE modem.

Integrated Generic Interrupt Controller (GIC): Allows flexible interrupt distribution and rapid interrupts between the processors.

Low-latency interrupt mode: An interrupt mode particular to the Cortex-R processor family which takes interrupts in as few as 20 cycles.

Asymmetric Multi-Processing (AMP): Whilst the Cortex-R7 supports Symmetric Multi-Processing (SMP), there is also provision for configuring the Quality of Service (QoS) within the SCU block such that each processor can have priority of access to a select range of memory and I/O addresses, and not be blocked by the other processor. This asymmetry is ideal for a system running two separate RTOS instances executing different programs, each with control over its own area of hardware and memory but with an occasional need to transfer data between them.

Overall, the new Cortex-R5 and R7 processors meet the demanding needs of LTE baseband systems being designed and ready for deployment this year and capable of supporting LTE-Advanced when it arrives. ARM has a long pedigree in processor design for real-time, deeply embedded applications with high performance and low power consumption, meeting the mobile industry's needs for generations. The Cortex-R4 processor is currently a very popular solution and is used in today's HSPA and first generation LTE devices. Cortex-R4 is licensed by 20 ARM Partners who are shipping it in products such as hard disk drive controllers, automotive electronic control units, medical equipment and mobile baseband. Now the Cortex real-time roadmap is filled out with Cortex-R5 and R7, there is a family of processors with performance and features sets addressing the widest range of high-performance real-time applications.



Figure 4: An ARM-powered USB modem