Hardware – Software Bring-Up Solutions for ARM v7/v8-based Designs

August 2015
Example ARM-based hardware/software system
ARMv8-based SoC software and verification challenges

- Multi-core early SW bring-up and integration on ARMv8 64-bit platform
- Bare-metal SW use case testing to verify multi-core cache and I/O coherency, concurrency, PSO, etc...
- Power profiling and analysis of real-world traffic
- Debugging of complex multi-core SoC SW scenarios on RTL sim/emulation platforms
- Integrating and verifying 100’s of IP blocks and SW from ARM, internal teams, and 3rd parties
- Characterizing and analyzing SoC performance and efficiently debugging issues
- Verification of IP blocks on AMBA interconnect w/ adherence to cache coherent (ACE) protocol

Development flow needs to support hardware/software integration and verification environments on multiple platforms.
Software is Key to verification

- Applications (Basic to Angry Birds)
- Middleware (Graphics, Audio)
- OS & Drivers (Linux, Android)
- Bare metal SW
- SoC in System
- System on Chip
- Sub-System
- IP

Time for critical bugs in System Environment to be removed

- Idea to spec
- RTL Becomes stable
- Only small gate level changes and ECO's
- Production
- Post silicon Validation

Spec | RTL-Design & IP Integration & Verification | IP Qualification | Netlist to GDSII | Fab | Post Si

Source: Cadence, IBS
ARM partnership to develop and deliver an ARM-based system verification solution

64-bit Multi-Core System Design Enablement
ARM & Cadence

- EDA Technology Access Agreement gives Cadence access to ARMv8 and ARMv7 processor IP, Mali™ GPUs, System IP and physical libraries
- First such agreement for ARM Cortex®-A50 processor series, based on the ARMv8-A 64-bit architecture
- Cadence to provide ARM-optimized tools and processes for the best power, performance, area (PPA)
- Will provide designers with easier SoC design, verification and implementation, helping to shorten time to market

“We are dedicated to empowering developers, designers and engineers to create valuable ARM technology and ensuring a fast, reliable route to market. The EDA technology and physical libraries resulting from this agreement will accelerate development of ARM’s most advanced technologies. We expect that this will be a tremendous benefit to developers of mobile devices, servers and the exploding market for everything in between.”

– Pete Hutton, executive vice president and president, Design Engineering, Cadence

Expanding the ARM-based System Verification Sol’n.

Reducing Time-to-Market for Mobile, Networking and Server Applications

- ARM®v8 64-bit and v7 32-bit Cortex® based embedded software development with Palladium Hybrid solution
- 10X faster SoC performance analysis and verification of ARM® CoreLink™ IP-based systems with Cadence Interconnect WorkBench
- Expanded Verification IP portfolio, adding support for ARM® AMBA® 5 CHI for all simulators & Palladium XP II

"In the ultra-competitive mobile, network and server markets, our partners are driven by the need to quickly differentiate and deliver the right product inside very tight development windows. The expanding collaboration between ARM and Cadence, and the availability of better ARM-based system design and verification automation, enables our joint partners to focus on innovation and getting their value added products to market faster.”

– James McNiven, deputy general manager, systems & software group, ARM

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Cadence Verification Solution for ARM® v8 SoCs

Palladium Hybrid for early SW bring-up and above-OS SoC validation
Perspec™ System Verifier SW-Driven use case verification
Palladium Dynamic Power Analysis profiling real traffic
Incisive Debug Analyzer synchronized embedded SW debug on ARM RTL CPU
SoC Workbench packaged v8 IP & VIP for rapid SoC integration & verification
Interconnect Workbench for SoC verification and performance analysis
VIP Portfolio w/AMBA ACE support on Incisive Simulation, Formal, and Palladium

Customer’s Application Specific Components
- 3D Graphics Core
- Modern
- Application Accelerators
- AES
- ...
Early OS and software bring-up Palladium Hybrid technology

Execute software at 100MHz
With standard or custom processor models

Plug-and-play integration with RTL
SoC-specific transactors and RTL I/F

Validate SoC + OS at 5-10MHz
High-performance memory coherency

Reduce SoC debug effort
System messages
Hardware/software debuggers
Close the HW/SW Concurrency Gap

Next Generation SW-Driven SoC Flow
- Continuous SW Development & Bringup
- Continuous System Validation
- HW Development & Verification

SW-Enhanced SoC Flow
- SW Dev On model
- SW Dev and Bringup On real HW design, Silicon
- System Validation
- HW Development & Verification

Traditional SoC then SW Flow
- HW Development & Verification
- SW Dev and Bringup on Silicon
- System Validation

Legend
- SW
- System
- HW

Powered By
Platform Hybrids
Emulation + Virtual Platform + FPGA

Enabled By
Virtual Platform
FPGA Prototype
Emulation

Tapeout
Silicon Samples
Product Ships
Virtual System Platform Use Models
Supported by same VSP System Creator License

Early SW Development
- High performance SW execution
- Run entire SW stack

SMP Linux boot:
- CPU0 615,093,547 instructions
- CPU1 489,558,519 instructions
- Total Instructions: 1,104,652,066
- In 30 seconds on a laptop computer
36 MIPS

SW Driver Validation
- Validate SW driver/firmware
- Running on the RTL

Key:
- RTL
- TLM
- SW

OS and above SW Validation
- Run entire SW Stack
- On RTL in Palladium for majority of SoC
Challenge is Modeling

• The Accuracy vs Speed trade-off
  – Direct Memory Interface (DMI) is key to virtual prototype performance: turn off DMI drop 100x in performance
  – To accurately model all memory transactions you must turn off DMI

• The Accuracy vs. Model Development time trade-off
  – Example modeling projects:
    – TLM 2.0 Loosely Timed Project: 45 models (Avg. time 2 staff weeks per model with a team of experience modelers)
    – TLM 2.0 Approximately Timed DDR Controller project: 1 model, 90% timing accurate (1.5 staff years with a team of experienced modelers)

• We found a better approach: Hybrid
  – Mixes Virtual Prototyping and RTL to get performance for software and accuracy for hardware
Early, High-Performance SW Execution on Palladium
Exclusive Solution combines the best characteristics of emulation and virtual platforms

TLM Virtual Platform – VSP
- Up to 100MHz
- Early Availability for SW Developers
- Advanced SW Debug
- Fast SW Turnaround Time

Emulation – Palladium® XPI/II
- Up to 4MHz
- From early-RTL to full-SoC Validation
- Advanced HW Debug
- Fast HW Turnaround Time

Hybrid Solution with SW Integrator
- Boot Complex OS at 48MHz
- Speed UP SW-Driven tests 1-10X over emulation
- Early Availability for SW Developers
- Advanced HW + SW Debug
- Fast HW and SW Turnaround Time
The Palladium/VSP Hybrid Solution

**Architected for SW Performance**
- High-speed virtual platform
- Asynchronous HW/SW Execution with Interrupt driven sync
- High-Speed Multi-Domain Memory Coherency

**Designed to integrate HW and SW flows**
- Does not require changes to HW or SW stacks
- Virtual connections into SW Engineer’s environments
- Seamless hybrid execution for both HW and SW users

**Proven Methodology, Unique Expertise**
- Cross-platform and design integration expertise
- Exclusive hybrid methodology delivers performance and repeatability
- Proven during successful application to SW-rich SoCs
A Different Hybrid - Palladium Hybrid Example

With virtual platform + Palladium turn-around time and debug

Run unmodified, Complex SW such as Android boot, OGL tests at FPGA speeds

Add Smart Memory: Patented TLM / RTL coherency

Add a minimal virtual model of your CPU sub-system

Connect using proven Technology, methodology

Use most accurate design model: RTL on Palladium
Hybrid Performance with SW Integrator
Compared to an All-RTL in Emulation Configuration

<table>
<thead>
<tr>
<th>Metric</th>
<th>All RTL in Palladium</th>
<th>Hybrid**</th>
<th>Increase</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linux boot (minutes)</td>
<td>30</td>
<td>0.5</td>
<td>60X</td>
</tr>
<tr>
<td>Android boot (minutes)</td>
<td>900</td>
<td>15</td>
<td>60X</td>
</tr>
<tr>
<td>Windows RT boot (min.)</td>
<td>1800</td>
<td>30</td>
<td>60X</td>
</tr>
<tr>
<td>512x512 2D test (min)**</td>
<td>30</td>
<td>2</td>
<td>15X</td>
</tr>
<tr>
<td># Emulation gates used</td>
<td>70 Million</td>
<td>40 Million</td>
<td>0.6X</td>
</tr>
</tbody>
</table>

* 70 million gate application processor, all blocks in Palladium®
** Virtualized CPU sub-system with register model of L1 & L2 caches. All other SoC blocks in Palladium.
*** Includes Linux boot, data preparation, image processing by HW engine and result checking. 1.3 million memory transactions. All boot numbers are full production images. Linux includes all drivers. Android and Win RT with SW rendering

Target Application
- Large, compute intensive SoCs

Target Users:
- HW-Dependent SW engineers,
- System validation engineers

Accuracy (see notes for details)
- SW: Delivers programmers-view accuracy
- HW: Full accuracy except for timing between virtual CPU and SoC fabric
- Memory: in fast mode, memory transactions are performed back-door. Thus, hybrid models not recommended for power or performance estimation
Customer’s Success with Hybrid
Global & Local customers
ARM use of Palladium XP platform for HW/SW co-design as part of the Cadence/ARM-based SoC solution

Results:
- 50X faster OS boot-up on ARM Mali™-T760 GPU
- 10X speed-up of overall hardware-software testing
- Shortened turnaround-time from hours to minutes

Technology:
- Palladium® XP Hybrid
- ARM Fast Models

“Early hardware-software co-development is critical in the design process for advanced, highly integrated projects. By using Cadence Palladium Hybrid technology to combine ARM Mali-T760 emulation with ARM Fast Models, we reduced the OS boot-up time, allowing us to run more extensive system-level software workloads and improve product quality.”

- Hobson Bullman, general manager, development solutions group, ARM
**ARM Mali - 2014**

High-Performance OGL-based GPU Validation

Results: 50X speedup in Linux Boot

- Reducing Time to Point of with Accelerated OS
  - Frank Schirmeister, Cadence
  - Robert Keje, ARM

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**OpenGL Validation**

- Successfully met project KOs for OpenGL ES 3.x
  - Executed and passed all 14K test cases by Tapeout
  - SW Stack ready for perf/w tuning on day 1
  - 4x faster than Palladium-only

**Performance Result**

- Linux kernel boot
  - Palladium only = 1 hour
  - Hybrid = 60 secs

- Android
  - Palladium only = Hours
  - Hybrid = 6 mins

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*By using Cadence Palladium Hybrid technology to combine ARM Mali-T760 emulation with ARM Fast Models, we reduced the OS boot-up time, allowing us to run more extensive system-level software workloads and improve product quality.*

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Palladium/VSP Hybrid with SW Integrator

- **Enable High-Performance execution of SoC SW with RTL**
  - Suitable for Bare Metal SW, OS, device drivers, test applications on OS
  - Full memory coherency
  - Boot Linux 30 seconds, run data-intensive SW at near FPGA speeds

- **Increase System Verification Productivity**
  - SW run-time reduced by 4-60X compared to standalone emulation
  - Run in simulation, emulation or hot-swap between the two
  - Reduce multiple debug iterations between SW and HW engineers
  - Reuse environments between SW development, HW Verification and system validation

- **Choose the right platform for your requirements**
  - Understand your speed vs. accuracy trade-off
    - Required to execute workloads
  - Understand modeling effort trade-offs
  - Utilize hybrid approaches