ARM’s Cortex®-M and Cortex-R Embedded Processors
ARM Cortex® Processors: Scalability for Every Market

Cortex-A Processors
- Rich OS
- Highest performance

Cortex-R Processors
- RTOS
- Fast response / real-time control

Cortex-M Processors
- DSP + MCU
- Smallest footprint / lowest power
ARM Cortex®-R Real-Time Embedded Processors

**Fast**: High processing performance at high clock frequencies

**Real-time**: Deterministic processing always meets real-time constraints

**Reliable**: Dependable with safety features and high error resistance

The real-time ‘workhorse’ with wide applicability
Tightly Coupled Memory for deterministic response
Memory Protection Unit

Dual core with accelerator coherency
Functional safety support

Extreme real-time performance, out-of-order execution
MultiProcessor Core with integrated interrupt controller
Cortex-R Series Summary

- 90+ licensees of ARM Cortex-R processors
- Many of the leading HDD and SSD storage manufacturers
- The leaders in mobile handsets for baseband processing
- The best in safety-critical industrial and automotive systems
- >2 billion Cortex-R processors shipped
ARM Cortex®-M Processor Family

**High Performance:** Low interrupt latency and fast bitwise operations

**Low Energy:** The most energy-efficient 32-bit processors

**Low Cost:** Low area, configurable with good code density

Lowest cost
Outstanding energy efficiency

Digital Signal Control (DSC) Processor with DSP
Accelerated SIMD Floating point (FP)

Maximum DSC Performance
Flexible Memory System
Cache, TCM, AXI, ECC
Double & Single Precision FP

'8/16-bit' Traditional application space

'16/32-bit' Traditional application space

Low power
Feature rich connectivity
Cortex-M Series Summary

- 280+ licenses of ARM Cortex-M processors
- Over 3,000 Cortex-M processor-based devices
- Implemented as ‘helper’ coprocessors in SoCs
- >10 billion Cortex-M processors shipped
ARM’s Cortex®-M7 and Cortex-R5 Processors
Cortex®-M7 Overview

- **Performance**
  - Achieving 5 CoreMark/MHz – 2000 CoreMark* in 40LP
  - Typical 2x DSP performance of Cortex-M4

- **Versatility**
  - Highly flexible system and memory interfaces
  - Designed for functional safety implementations

- **Scalability and compatibility**
  - Enables simple migration from any Cortex-M processor
  - Widest third-party tools, RTOS, middleware support

*CoreMark 1.0: IAR Embedded Workbench v7.30.1 --endian=little --cpu=Cortex-M7 -e -Ohs --use_c++_inline --no_size_constraints / Code in TCM - Data in TCM
Cortex®-M7 Partner News

- **Atmel**
  - Launched new SAM70 series based on Cortex-M7 (300MHz)
  - First devices have up to 384kB SRAM and 2MB Flash, AXI connection to large external memories
  - Targeting Automotive, IoT and Industrial

- **freescale**
  - Launched Kinetis KV5x family based on Cortex-M7 at Embedded World 2015
  - Now in preproduction, devices later this year
  - Targeting advanced motor control and power conversion

- **STMicroelectronics**
  - Launched full STM32F7 family of processors, now available to mass market
  - 1MB Flash, 320kB SRAM, AXI connection to large external memories, 216MHz
  - Targeting Audio, Home Automation, Medical, Industrial, Motor control
  - Roadmap to faster devices on smaller process technology (400MHz)
Cortex®-M7 Target Applications

- High-end member of existing Cortex-M based MCU family
- Replacement for MCU + proprietary DSP
- Powerful sensor hub, capable of voice recognition, image processing
- Powerful processor for factory automation: motor control, PLC, servo control
- Flexible processor for automotive: dashboard, ABS, low-end gateway, transmission, convenience electronics
Cortex®-M7 Key Features (1)

- High performance core with DSP capabilities
  - Six-stage dual-issue pipeline
  - Powerful DSP instructions and SP/DP Floating Point
  - **Best-in-class core for high-end MCU, or replace MCU+DSP with Cortex-M7**

- Flexible, memory system
  - Tightly-coupled memories for real-time determinism
  - 64-bit AXI AMBA4 memory interface with I-cache and D-cache for efficient access to external resources
  - **Enables MCUs to be built with access to large external memories and powerful peripherals**
Cortex®-M7 Key Features (2)

- **ARMv7E-M architecture**
  - 100% binary forwards compatibility from Cortex-M4
  - Key Cortex-M family processor characteristics: Ease of use, excellent interrupt latency
  - **Fast interrupt response for real-time systems, reuse code and system design from existing products to reduce development costs**

- **Safety features**
  - Memory ECC (SEC-DED), MPU, MBIST, lock-step operation, full data trace, safety manual
  - **Enables entry into safety-critical markets.**
Cortex®-M7 has the same powerful instruction set as Cortex-M4:
- Integer MAC instructions are all single-cycle
- SIMD instructions can work on 8-/16-bit quantities packed in to a 32-bit word
- Arithmetic can be signed/unsigned, saturating/non-saturating
- A few new FP instructions for FPv5
- Results are geo-mean of EEMBC IPC relative to Cortex®-M4 baseline
- Comparable memory systems – zero wait state memory for Cortex-M4, caches for M7
- Same process technology

<table>
<thead>
<tr>
<th>Category</th>
<th>Cortex-M7</th>
<th>Cortex-M4</th>
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<td>FPMark (SP FP)</td>
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<td>Networking</td>
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<tr>
<td>AutoIndy (Int)</td>
<td>1.96</td>
<td>1</td>
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</table>

At max Cortex-M7 frequency

At maximum Cortex-M4 frequency
Cortex®-M7: Competitive with Popular DSPs

- Essential DSP features
  - Parallel execution of loads, stores and MAC
  - SIMD support, single-cycle MAC
  - Single and double precision floating point unit
  - Minimal loop overhead (branch predictor/BTAC)
  - Optimised DSP libraries

Consistently good performance across key DSP functions

<table>
<thead>
<tr>
<th>Normalized cycles, lower = better</th>
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<tbody>
<tr>
<td>Biquad Cascade</td>
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<td>FIR Filter</td>
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<tr>
<td>Real FFT</td>
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<tr>
<td>Complex FFT</td>
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</tbody>
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- Cortex-M7
- 32-bit DSP E
- 32-bit DSP F
Cortex®-M7 – Replacement for MCU+DSP

**Trends:**
- Convergence of MCU+DSP to DSC for cost reduction
- Increased processing demands
- Increasing consumer expectation of quality in portable devices

**Example applications:**
- Multi-channel audio / Dolby Audio
- Advanced Motor Control
- Factory Automation
- Automotive
- Image processing
- Power conversions

**Cortex-M7 Advantages:**
- High performance core with fast DSP
- Compatibility with existing Cortex-M4 designs
- Flexible memory system
Enabling More Capabilities for Feature-Rich Devices

2x More performance delivering improved flight management

Cortex®-M7
400 MHz

Cortex-M4
168 MHz

Finer degree of control
Accurate speed measurement
Finer GPS accuracy
Secure telemetry radio

Source: 3D Robotics, PX4 autopilot ETH Zurich
Helping Drive Richer Audio Experiences

2x More performance delivering advanced sound processing

Cortex®-M7 160 MHz
- Dolby Digital Plus (with post processing)
- 7.1 Multi-channel audio support
- More speaker EQ processing
- Capacity for decoders
- More connectivity options

Cortex-M4 130 MHz
- Dolby Digital
Cortex®-M7 in Automotive

- **Trends and challenges:**
  - Safety certification mandated in more regions
  - Convergence of functionality into fewer MCUs/ASSPs
  - Increasing user requirements and expectations

- **Typical Applications**
  - Dashboard in medium-range cars
  - Voice recognition (for Multimedia control functions)
  - Character recognition (eg Kanji)
  - “Convenience” features (eg intelligent headlight clusters)
  - Chassis, electric power steering, “steer-by-wire”
  - Automotive audio

- **Cortex-M7 Advantages:**
  - High performance core with fast DSP
  - Safety features built in and safety manual
  - Determinism with high performance
  - Full trace via ETM
Cortex®-M7 in Industrial Control

- **Trends and challenges**
  - High performance control functions
  - Safety, reliability and conformance will become mandatory
  - 80-90% of cost is software, Cortex-M offers scalability and protects software investment

- **Typical applications:**
  - Factory Automation
    - Inverters, Servos
    - Programmable Logic Controllers
    - High-speed comms
  - Intelligent motor control

**Cortex-M7 Advantages:**
- Increased DSP performance for control functions
- Safety features built-in
- In-order pipeline gives performance with predictability
- TCMs and low interrupt latency: Interrupt response within 100ns required
- Scalability from Cortex-M3 through Cortex-M7 up to Cortex-A53
Cortex®-R5 Processor
Enhanced SoC integration with Low Latency Peripheral Port, Accelerator Coherency Port

- Fast high performance 1.66 DMIPS/MHz
  - Energy-efficient, eight-stage dual-issue pipeline
  - ARMv7R architecture - Thumb-2 / ARM instructions
  - Hardware divide, SIMD, SP or SP/DP FPU option
  - Harvard caches, 64-bit AMBA AXI-3 bus

- Deterministic and fast interrupt response
  - Unified Tightly-Coupled Memory system
  - Low Interrupt Latency microarchitecture

- Reliable with fault handling built into core
Cortex®-R5 Hardware Overview

- Vectored Interrupt Controller port
- Tightly-Coupled Memory port A for RAM, ROM or Flash
- Unified TCMs hold both code and data
- Tightly-Coupled Memory port B for RAM, ROM or Flash
- Ports B0 and B1 allow processor accesses to commutate with AXI-S accesses
- Data I/O for TCMs
- Optional memory protection unit
- Optional floating point pipeline
- Cortex-R5 low-latency peripheral ports with AHB option
- Harvard instruction and data caches
- Cortex-R5 accelerator coherency port option maintains D-cache contents for external DMA I/O

- Synthesis config: Caches, TCMs, AXI-S, FPU, MPU, break/watch-points, ECC/Parity, lock-step
- R5 only: ACP/µSCU, AHB-LLPP, SP-only FPU, split-lock

CoreSight debug with full instruction and data trace
Cortex®-R5 Bounded Real-Time Response

- **Superscalar execution throughput**
  - Cache line buffers minimise stalling while waiting for L2 memory system

- **Low Interrupt Latency mode**
  - Fast interrupt response abandons pending and restartable memory operations

- **Tightly Coupled Memory**
  - Static Level-1 memory system for locally held code and data e.g. Interrupt service routines

- **Low Latency Peripheral Port**
  - Introduced in Cortex-R5
  - Direct paths to LSU and store queue avoid delays in caches and AXI-Main
Safety in Embedded Processors
Reliability Requirements in Wider Range of Embedded Systems

- Traditional markets
  - Automotive
  - Industrial Control

- Emerging markets
  - Infrastructure / Smart Cities
  - Medical
  - Home gateway / communication infrastructure

- Increasing reliance on embedded systems to continue functioning when errors occur

- Higher chance of errors at advanced nodes, in larger memories and in bigger programs
Typical Technical Requirements

- Reducing the possibility of errors
- Detection of errors
- Correction of errors
- Robustness – reducing single points of failure

Memory

Logic

Software
Cortex®-M7 Functional Safety Support
Cortex®-M7 Support for Functional Safety
In accordance with ISO 26262, IEC 61508 etc.

- Cortex-M7 incorporates fault detection and control features
  - ECC for detection and correction of random faults in cache RAMs
  - Dual-Core Lock-Step option detects random faults in processor logic
  - Memory Protection Unit to detect systematic faults in software
  - On-line MBIST interface allows scrubbing of memory for errors whilst applications are running

- Features necessary for microcontrollers targeting automotive and industrial applications

- Safety Package will be released later in 2015
Cortex®-M Processor Features to Support Reliability

- Fault exceptions
  - HardFault (available on all Cortex-M processors)
  - Configurable faults on ARMv7-M architecture: Usage Fault, Bus Fault, Memory Management Fault
- Non-Maskable Interrupt (NMI)
  - Highest priority exception
  - Watchdog / BOD (Brown Out Detection)
  - Cannot be disabled
- Memory Protection Unit (MPU)
  - Use by RTOS to configure memory access permissions and memory attributes
  - Optional, programmable
Example – Stack Protection

- Stack overflow is a common cause of embedded system failure
  - Software developer’s mistakes
  - Unforeseeable workload

- Detection methods at runtime
  - Use MPU to define accessible RAM space
  - Stack limit by placement
  - Use stack checking feature in RTOS
    (Checks at context switches and/or OS ticks)
ECC on TCM Interfaces

- **Tightly Couple Memory (TCM) interfaces support optional ECC**
  - ECC scheme defined by chip designers
  - RETRY and ERROR signals

- **RETRY signal**
  - Assert 1 cycle after read data
  - Give ECC logic chance to correct data

- **ERROR signal**
  - After retry, if error cannot be corrected
  - Result in bus fault exception
Cache ECC Support

- Handled internally inside Cortex®-M7 processor
  - Optional
  - ECC initialized as part of cache invalidate during cache enabling
  - Cached data is **corrected on the fly with clean and invalidate**
  - Un-correctable errors trigger fault if in data cache & dirty (Instruction and clean data can be discarded)
- I-Cache, D-Cache error bank registers
  - Indication of cache memory error locations
  - Cache lines can be locked down to prevent them from being used
- Additional signals for cache error monitoring / handling
Dual Core Lock Step Support on Cortex®-M7 Processor

- Duplicate logic only
  - Cache and TCM are protected by ECC
  - Outputs are compared
- Skewed operation to prevent common mode failures
- Potentially can use different logic implementations between the two
  - Prevent common mode failures
  - Lower power implementation for redundant logic (not in critical path)

Example DC-LS, customers can modify top level comparators
Cortex®-M7 Safety Documentation Package contents

- Essential documentation to support designing Cortex-M7 products for safety-related markets
- Three key documents within the Safety Documentation Package:

  - Safety Manual
    - Overall description of functional safety activities within ARM
    - Product specific aspects of functional safety
    - Overview of safety architecture
    - Description of fault detection and control mechanisms
    - Summary of safety analysis results

  - Failure Modes and Effects Analysis Report
    - Block and sub-block level partitioning
    - Estimated failure rate distributions
    - Sample quantitative analysis

  - Development Interface Report
    - Identification of safety-lifecycle aspects applicable to ARM and IP integrator
Cortex®-R5 Functional Safety Support
### Dependable Systems with Cortex®-R4/R5

- **Cortex-R4/R5** have many features to enable safe processing
  - Cortex-R5 has optional Safety Documentation Package

- **Memory Protection Unit** detects unauthorized address accesses

- Data and address protection integrated within processor architecture
  - ECC or Parity on Level-1 memories. Parity on selected busses
  - Cortex-R5 has extended ECC support to all AXI and AHB busses, incl. ACP

- **ECC** offers advanced Single Error Correction or Double Error Detection
  - Automated memory error correction integrated into processor pipeline
  - Support for external ECC logic, e.g. in a Flash memory controller

- Processor incorporates error counting and logging for diagnostics

- Optional redundant core configuration for lock-step operation
  - Cortex-R5 allows static switching between lock-step and twin core operation
ARM Compiler 5 Support for Functional Safety

- Compiler Safety Package for software development in safety markets
  - Industrial control, automotive, medical, transportation, military and others

- Access to the Safety Package provided with DS-5 Ultimate and Keil MDK Pro
  - Valid DS-5 or MDK support and maintenance entitlement enables extended maintenance
  - Compiler installation is an add-on to the standard product installation

**Qualification Kit**
- Development process docs
- Safety manual
- Defect report
- Test report

**Extended Maintenance**
- Five year commitment
- Technical support
- Critical defect fixes

**Functional Safety Certified**
- TÜV SÜD certification
- ISO 26262 (ASILD)
- IEC 61508 (SIL3)
ARM Cortex®-M and Cortex-R Embedded Processors

**Cortex-M**
- **Cortex-M4**: Mainstream Control & DSP
- **Cortex-M7**: Maximum Performance Control & DSP
- **Cortex-M0**: Lowest cost, Low power
- **Cortex-M0+**: Highest energy efficiency
- **Cortex-M3**: Performance efficiency

**Cortex-R**
- **Cortex-R7**: High performance
- **Cortex-R4**: 4G modem and storage
- **Cortex-R5**: Functional safety package
- **Cortex-R5**: Real-time standard
Thank You

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