ARM Product News Summary

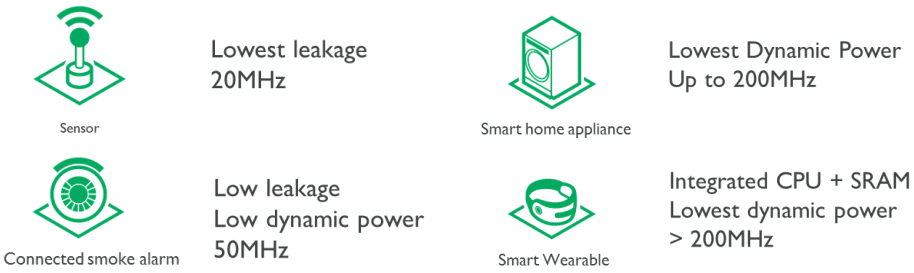
ARM Artisan IoT POP IP provides an optimized implementation path to low-power IoT silicon

Highlights

- Innovative logic and memory architecture features that minimizes area, leakage and dynamic power while optimizing performance
- Silicon-proven physical IP that works seamlessly with latest ARMv8-M processors and system IP
- Power implementation solutions for various IoT applications that can maximize battery life

Balancing power and performance

Teams designing an SoC implementation for IoT face a number of challenges due to the market's specific requirements. SoCs must be low cost, maximize battery life and have the ability to be customized for a variety of end applications. Trying to balance the various power requirements in the different parts of the system is a non-trivial task, and ARM® Artisan® IoT POP™ IP is meant to guide and help accelerate that process and speed the time to tape out. IoT applications can vary in their performance and power requirements:



Product overview

ARM IoT POP IP helps accelerate the implementation of IoT SoCs by offering physical IP as well as reference designs and know-how to develop a design that has optimal performance with minimum area. The IoT POP includes implementation solutions that take into account the power budget that is needed not just for the CPU, but the rest of the system, including the Always on Subsystem that require a minimum amount of leakage power. The ultra low power nature of the process technology helps to address the wide variety of energy or power needs for the variety of IoT applications that exist.

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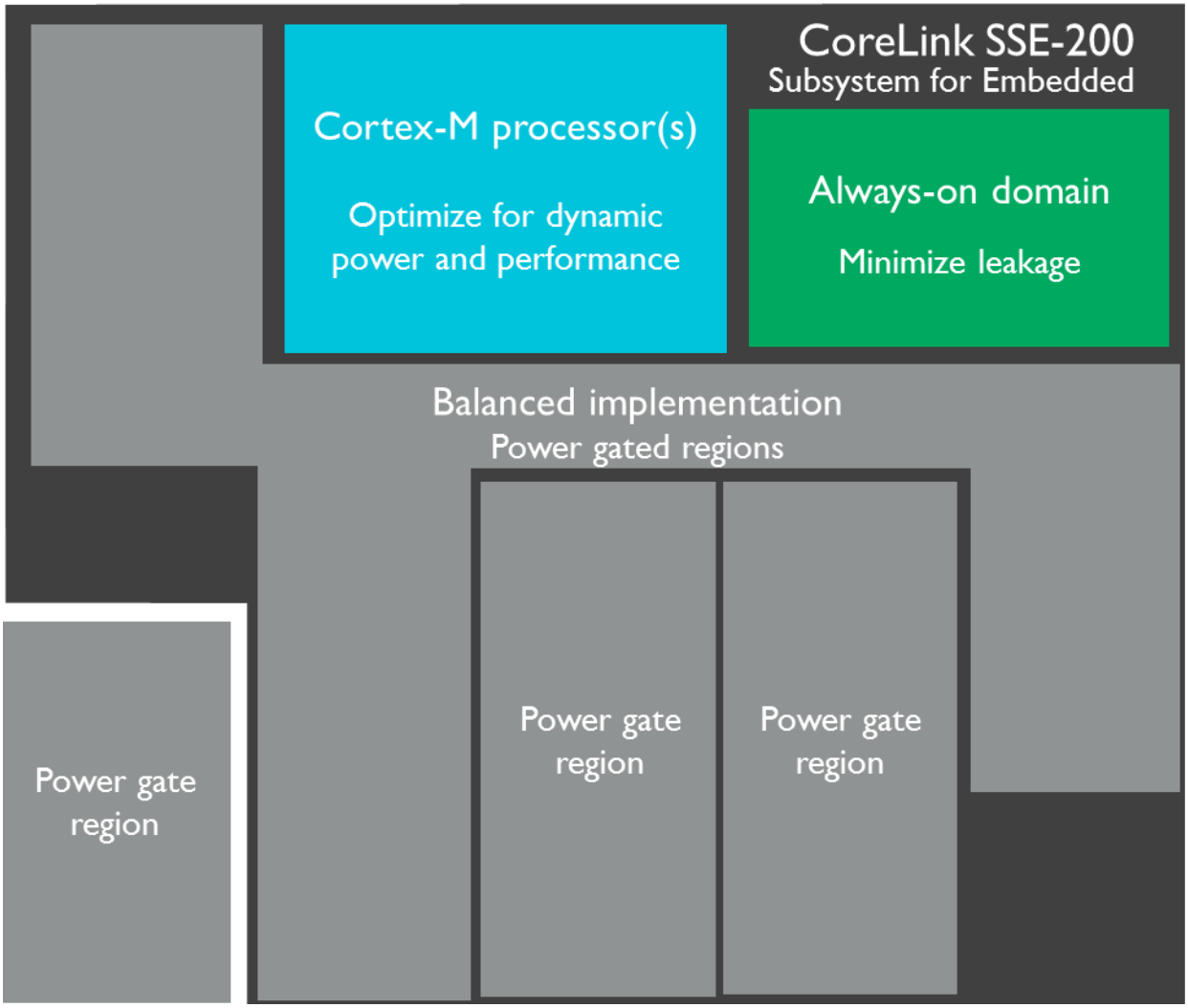
To further simplify customers that develop with Cortex-M33, the IoT POP IP has been designed for use with the CoreLink SSE-200 subsystem, with a very easy-to-use reference design that outlines the physical IP that is needed, along with the implementation methodologies that provide the appropriate power profile that is needed for a particular IoT design.



- Seamless integrated physical IP package for Corelink SSE-200 supporting Cortex-M33 at TSMC 40ULP process node
- Various power profile reference flows with major EDA tool support
  - Includes CPU element sub-block at different performance / power envelopes to support sub-block implementation within CoreLink SSE-200
  - CPU element combined with SRAM element– focused for high end / high frequency implementation.
  - System Control element with emphasis on <1uA logic power consumption.
  - User guide and datasheets for 5 trial implementations ; docs to explain power domains and assumptions and SoC guidelines.

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ARM Artisan TSMC 40ULP Logic Platform

Cell Architecture	Products	Vt / Channel Length	Voltage Domains (+/-10%)
SC7MC	Base, HPK, HDLPK	SVt c40/c50, LVt c40/c50, eLVT c40/c50, eHVt c50	1.1V 1.0V 0.9V
	PMK	eHVt c50 , SVt c40-c50, SVt-eHVt c50	
	ECO	SVt c40	
SC9MC	Base, HPK, HDLPK	SVt c40/c50, LVt c40/c50, eLVT c40/c50, eHVt c50	
	PMK	eHVt c50 , SVt c40-c50, SVt-eHVt c50	
	ECO	SVt c40	
SC11 TGO	Base, PMK	SVt	3.3V, 1.1V, 0.9V

ARM Artisan TSMC 40ULP Memory Platform

Memory IP	Periphery	Voltage Domains (+/-10%)
Ultra Low Power SP-SRAM Compiler	SVt-SVt SVt-eHVt	1.1V 1.0V 0.9V
Ultra Low Power SP-RF Compiler	SVt-SVt SVt-eHVt	
Ultra Low Power Programmable Via-ROM	SVt-SVt	