Overview
The ARM VSTREAM™ enables the connection of software debug tools, such as the ARM Development Studio 5 (DS-5™) debugger and the RV Debugger, to ARM processors running RTL on simulators and hardware emulators.

Key Features
- Software Debug Connection to RTL Simulators and Emulators.
- Early integration and functional validation of ARM processor-based SoCs.
- High-speed software download and processor control.
- Convenient and easy to set up software solution.
- Integrated multicore and multi-processor support.
- Post-process PTM™ or ETM™ instruction trace.
- Reduced setup time due to virtual debug connections, eliminating the need for JTAG debug hardware.

Supported EDA Tools

<table>
<thead>
<tr>
<th>RTL Simulators</th>
<th>Hardware Emulators</th>
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<tbody>
<tr>
<td>Cadence Incisive</td>
<td>Cadence Palladium</td>
</tr>
<tr>
<td>Mentor ModelSim</td>
<td>Eve ZeBu</td>
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<tr>
<td>Mentor Questa</td>
<td>Mentor Veloce</td>
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<tr>
<td>Synopsys VCS</td>
<td></td>
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</tbody>
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ARM works closely with EDA vendors to develop, integrate and validate VSTREAM transactors for their EDA tools-flow.

Accelerate SoC Integration and Validation
Processor run-control and system visibility on RTL simulators accelerate SoC integration, functional validation and early software development. With VSTREAM it is possible to stop the processor, control software execution with breakpoints, view and modify processor/co-processor registers, and validate memory accesses.

VSTREAM implements a SCE-MI 2.0 or ZEMI-3 transaction-based connection into a CoreSight Debug Access Port (DAP). This connection enables significantly faster software download speeds (~400KB/s) and debugger responsiveness on emulators.

The co-emulation transactor based connection replaces conventional JTAG debug hardware connections to emulators. This results in greatly reduced setup time and makes it very flexible for instantiating multiple software debugger connections to emulators running several designs in parallel.

With VSTREAM it is possible to download a Linux kernel image to an emulator in a matter of seconds, and single-step through the code at up to five steps per second. By delivering debug speeds comparable to final silicon, VSTREAM greatly improves the efficiency of emulator time.
VSTREAM Transactors

A debug session with VSTREAM is equivalent to one with JTAG probe connected to a hardware target, since they both use the parallel debug port of Cortex™ processors.

However, VSTREAM is significantly faster on emulators, as it provides a 32-bit parallel interface direct into the CoreSight Debug Access Port. VSTREAM bypasses the slower JTAG interface, implementing SCE-MI 2.0 or ZEMI-3 pipes instead.

VSTREAM provides standard, future-proof debug access to Cortex processors, independent of their pipeline, memory management unit, and cache system.

ARM Software Debugger Features

- Processor Run Control enables run, stop, set breakpoints, single step through source and assembly code, and reset processor.
- Processor Views monitor and change active and banked processor and co-processor registers.
- Memory Views show the contents of memory from the processor’s point of view as characters, integers, instructions, or floating point values.
- Software Views enable the debug and validation of boot code, kernel, and drivers. They include C/C++ source matching disassembly, and variable views.
- Command Line Interface supports high and low level debug commands to the processor or directly to the CoreSight Debug Access Port.
- PTM or ETM instruction trace helps to get a history of instructions executed by the processor.

Client/Server Architecture

VSTREAM supports remote access via TCP/IP from the workstation running the software debugger, to the workstation that is running the EDA tools. VSTREAM can be instantiuated multiple times to seamlessly connect several debuggers to several designs running on a single emulator or simulator workstation.