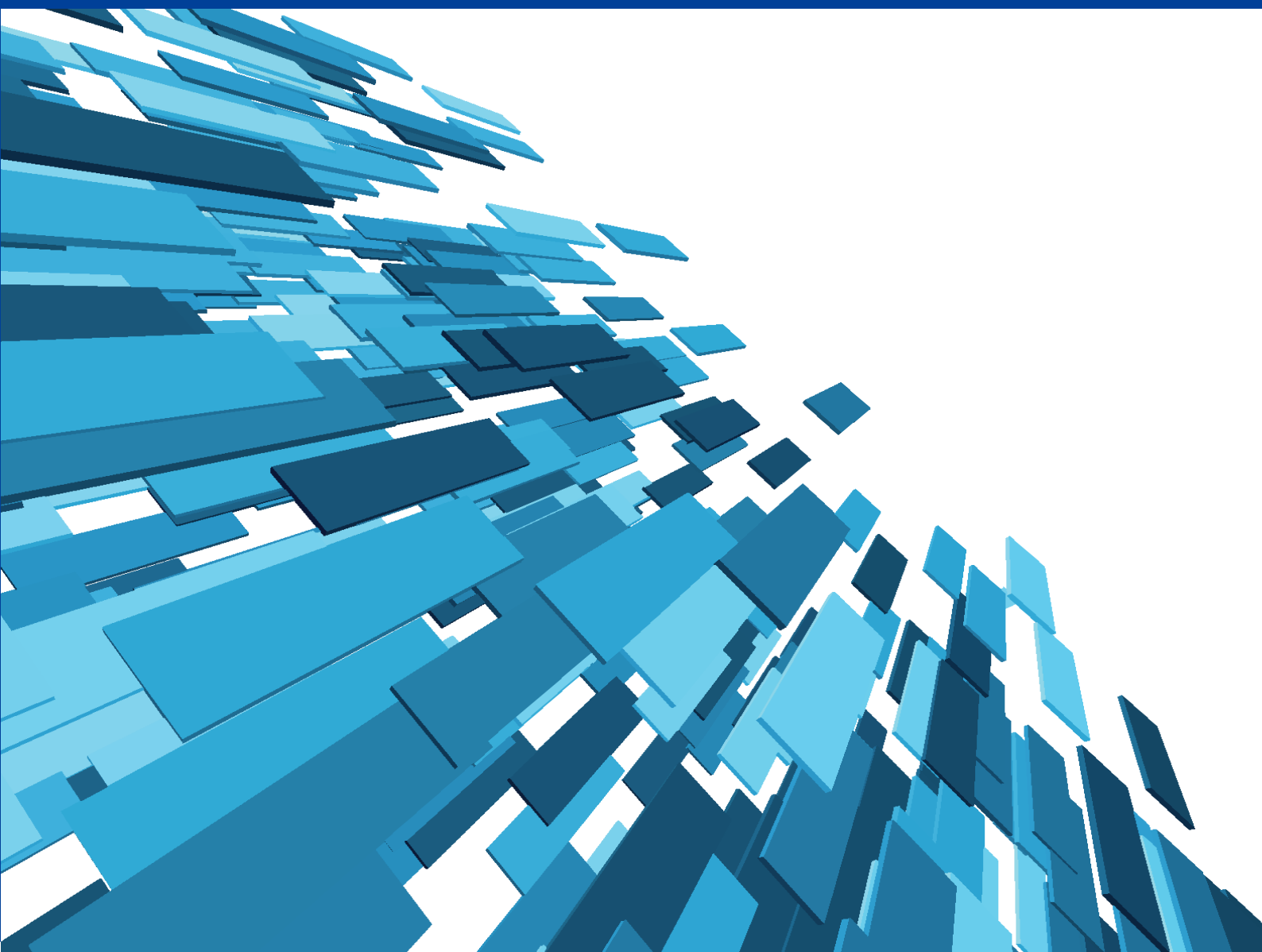


# Heterogeneous Multi-Processing Solution of Exynos 5 Octa with ARM<sup>®</sup> big.LITTLE™ Technology



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## Abstract

With an increasing need for higher performance in mobile devices, the battery capacity must be increased accordingly, which is not easy because of the small size of mobile devices. Therefore, the demand for better power efficiency of mobile devices, which implies lower power consumption and higher performance is becoming critical. Recently, big.LITTLE architecture was introduced to fulfill the demand. A few solutions are available to be implemented in the big.LITTLE architecture. This paper introduces Heterogeneous Multi-Processing (HMP) solution that is more power-efficient than the cluster switching solution ported in several mobile devices in the current market.

## Introduction

Mobile CPU had evolved by increasing the CPU clock frequency to enhance the performance. This approach faced the peak clock frequency limit barrier, above which power consumption increases exponentially. Then, the approach has evolved from increasing the CPU clock frequency to building the multi-core architecture.

Despite the controversy over the necessity of multi-core architecture, current mobile devices operate on the multi-core platform to achieve higher performance. The dual-core architecture was adequate for mobile devices, however, quad-core platform seems to be the standard. Therefore, the issue of quad-core has to be shifted to increasing the power efficiency rather than multi-core architecture itself. This is because mobile devices have limited power, and the end user uses it more closely than the PC. Therefore, the thermal issue is more critical in mobile devices than the PC.

To improve the power efficiency and achieve higher performance simultaneously, big.LITTLE architecture had been introduced. Samsung has implemented the big.LITTLE technology to achieve higher power efficiency with the multi-core performance.

big.LITTLE architecture consists of these cores in single silicon:

- Performance driven big core
- Power efficiency driven LITTLE core

The first and simplest implementation of big.LITTLE architecture is the cluster switching mode. In the cluster switching mode, activation and deactivation is performed per cluster. Therefore, only one cluster is active at a time, while the other cluster is in inactive mode. All tasks are assigned one cluster even if power and performance requirement of all tasks are not same. Therefore, there is less flexibility and efficiency for power and performance. To fully maximize the big.LITTLE architecture, HMP solution is implemented with full flexibility and efficiency.

Exynos 5 Octa processors include octa-cores and cluster switching. These were selected initially to secure a reliable solution for the newly-adopted architecture. Finally, HMP solution has been implemented to provide higher performance with a balance of well-tuned operations, under the same thermal and power consumption with reliability.

## Operation of big.LITTLE Modes

In the big.LITTLE architecture, big cores and LITTLE cores have different characteristics. For example, big core provides higher performance, and LITTLE core provides better power efficiency.

Therefore, the big core delivers higher performance but consumes more power, whereas the LITTLE core delivers more power efficiency but delivers lower performance. Various operation modes including the cluster switching mode and HMP mode operate these cores with different characteristics in single silicon. The sub-sections describe the operation of these two big.LITTLE operation modes:

- big.LITTLE Cluster Switching Mode
- big.LITTLE HMP Mode

### Operation of big.LITTLE Cluster Switching Mode

In cluster switching mode, big cluster consists of identical big CPU cores such as Cortex™-A15. The LITTLE cluster consists of identical LITTLE CPU cores such as Cortex-A7. All tasks are assigned to one cluster and the other cluster is deactivated. When the workload of tasks reaches to a pre-defined workload threshold, all the tasks are switched to the cores in the next cluster, and the previous cluster is deactivated. It is flexible because both clusters do not have to include identical number of cores, unlike the CPU migration mode which requires identical number of cores in both clusters. Therefore, it is possible to reduce the number of big core less than LITTLE core in the cluster switching mode. However, since it works as cluster unit, all the tasks are assigned one cluster even if all tasks have different power and performance requirements, and it makes cluster switching mode less flexible and less efficient than HMP mode.

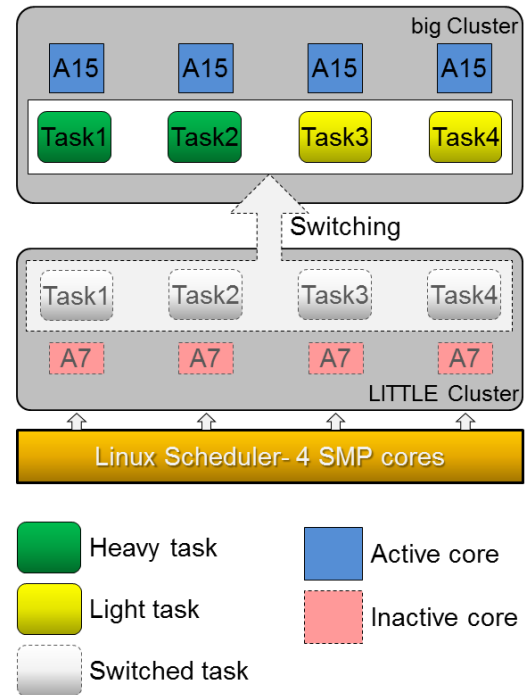


Figure 1 : Operation of big.LITTLE Cluster Switching Mode

### Operation of big.LITTLE HMP Mode

big.LITTLE HMP mode is the most sophisticated and flexible mode in the big.LITTLE architecture. In this mode, activation and deactivation is performed per core irrespective of the cluster, therefore each and every CPU core can be independently activated or deactivated according to the required workload. In other words, all tasks are assigned to the appropriate core according to the power and performance characteristics of the task. It indicates that highest performance can be utilized at the highest workload because all cores in both clusters can be activated simultaneously. In addition, power efficiency can be maximized for all types of workload because all tasks can be assigned to appropriate cores according to each task's different power and performance characteristics.

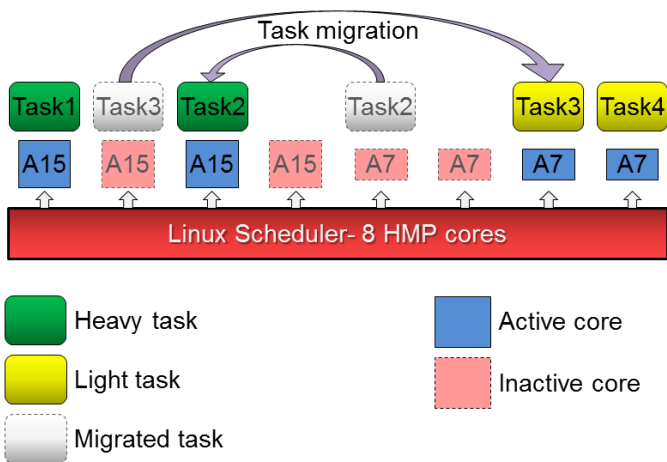


Figure 2 : Operation of big.LITTLE HMP Mode

Compare Figure 2 with Figure 1 for example, four big cores are activated in the cluster switching mode in Figure 1, while two big and two LITTLE cores are activated in the HMP mode with same tasks characteristics as illustrated in Figure 2. Therefore, it is obvious that HMP mode is the most power efficient solution for mobile CPU.

## Benefits of HMP Solution for Exynos 5 Octa

Unlike other modes of big.LITTLE architecture, HMP solution does not have the limitation about core or cluster. In addition, HMP solution can manage with change of power and performance characteristic of running tasks. Therefore, all the running tasks can be reallocated to other core in another cluster in the middle of task running according to the change of performance and power requirement of the task. Therefore, this utmost flexibility facilitates HMP mode to achieve both performance improvement and power efficiency.

	Cluster Switching	HMP Mode
Configuration	One cluster is activated at a time	All cores work independently
Kernel Impact	Minimum modification on Linux kernel	Linux Scheduler & CPU driver should be modified
Max Performance	Sum of performance of all the big cores	Sum of performance of all the big and LITTLE cores
Switching / Migration	Switched by CPU frequency framework	Migrated by Scheduler

Table 1 : Comparison Between Cluster Switching Mode and HMP Mode

As described in the above paragraph, HMP solution of Exynos 5 Octa provides highest flexibility and efficiency for the performance and power that is essential to the mobile CPU. In the HMP solution, each and every core can be activated, and it indicates that any core with no running task can be deactivated. In the lowest workload case, only a single LITTLE core runs at the lowest operable frequency, while other cores are deactivated. If there are multiple tasks which require that some tasks should be executed on the big cluster, while others should be executed on the LITTLE cluster, then all the tasks can be assigned to appropriate cores irrespective of the cluster. However, in the cluster switching mode, all the tasks are assigned to the big cluster in same case. Therefore, power efficiency can be fully maximized. The most powerful operation also can be performed by all cores running at the same time at the heaviest workload case.

Besides the HMP architecture, which is the most sophisticated and powerful use model of big.LITTLE architecture, software implementation and optimization are another essential factors to maximize the benefits of HMP architecture. The scheduler must allocate the task to the appropriate core, and migrate to the appropriate core at the correct time. Various in-depth analysis and investigation about core and task operation, and tuning have been performed to achieve improved performance and efficiency.

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To achieve performance and power efficiency simultaneously, the profiling and analyzing of various user scenarios with various performance and power requirements were required. The following sub-section describes the improved result of HMP solution.

### Experimental Data of HMP Solution

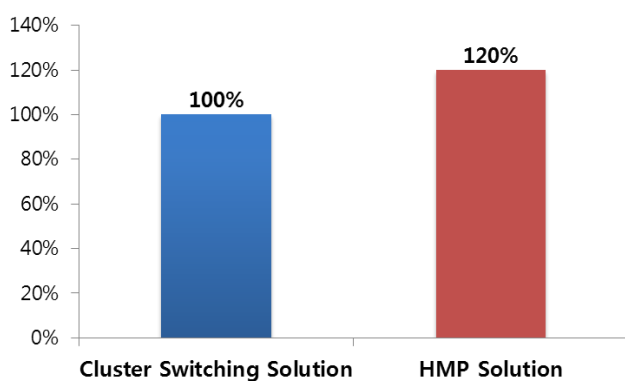


Figure 3 : Performance Improvement on HMP Solution of Exynos 5420

It has been measured by running Geekbench 3 benchmark from Exynos 5 Octa reference board to check CPU score. The benchmark result shows an improvement in HMP solution as compared to cluster switching mode. Thanks to the flexible HMP architecture and accurate scheduler that can efficiently manage widest range of workload, HMP solution of Exynos 5 Octa provides 20 percent improved performance when compared to cluster switching solution with same hardware specification. Even with higher performance than cluster switching mode, HMP solution shows similar power consumption compare to cluster switching mode. Various scenarios were investigated for power consumption comparison including Home Screen, 720p playback, 1080p playback, 3D game and BBench. Most scenarios reveal similar power consumptions in both cluster switching mode and HMP solution. Scenarios such as 3D game show less power consumption in HMP solution.

### Conclusion

This paper introduces various big.LITTLE solutions and describes the advantage of HMP solution, and its superiority among the other big.LITTLE modes such as cluster switching solution.

The test results derived from an Exynos processor platform reveal that HMP solution of Exynos 5 Octa can deliver real value to end users by leveraging on the octa-core CPU in Exynos processors.

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## References

- [1] HyunDuk Cho, et al. "Benefits of the big.LITTLE Architecture", EETimes, Feb 2012. [online], Available : <http://www.techonline.com/electrical-engineers/education-training/tech-papers/4236398/benefits-of-the-big-little-architecture> [Accessed 29th Oct. 2013]
- [2] Robin Randhawa, "Software Techniques for ARM big.LITTLE Systems", ARM, Apr. 2013. [online], Available : [http://www.arm.com/files/downloads/Software\\_Techniques\\_for\\_ARM\\_big.LITTLE\\_Systems.pdf](http://www.arm.com/files/downloads/Software_Techniques_for_ARM_big.LITTLE_Systems.pdf) [Accessed 29th Oct. 2013]

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