Driving with ARMv8-R Architecture

from Mobile to Automobile

Chris Turner October 2013

Foreword
ARM processors are increasingly used in automotive applications such as In-Vehicle Infotainment (IVI), Advanced Driver Assistance Systems (ADAS), powertrain, chassis and body control. Moreover, there are emerging opportunities in Vehicle-to-Vehicle and Vehicle-to-Infrastructure (V2V, V2I) communications which further extend the scope and sophistication of computation systems in vehicles of the future.

These developments are driving the next generation of automobile electronics where more use of ARM processors is made each year. This paper discusses the technology behind some of these applications and describes where and how ARM processors are used in automotive electronics and associated highways infrastructure applications. The paper then introduces the evolution of ARM processor architecture for real time control and safety systems, enabling designers to manage the increasing complexity of automotive hardware and software, including those systems concerned with functional safety. Future ARM-powered products implementing this new architecture will also offer enhanced real time performance and contribute towards improved software quality and reliability with increased code re-use and portability.

Progress in Automotive Electronics
Electronics have become very important to modern automobiles and the features they support are now a key factor in customers’ purchase decisions. In fact, much of the legislation concerning vehicle emissions and safety could not be delivered in any practical way without the help of modern electronics. However, electronics have also become a significant contributor to vehicle cost and development time.

Most electronically-enabled features in modern automobiles can be classified as follows:

**In-Vehicle Infotainment:** The car radio, media player, hands-free telephone (Bluetooth), satellite navigation and general user interface. Usually incorporating a large display, user interface and possibly voice activated. This user-facing electronic system is often a key differentiator for the modern customer

**Instrument cluster:** The traditional, and obligatory, speedometer and odometer are almost always facilitated with electronics now, together with the revolutions counter, fuel and temperature gauges and other driver interfaces. The cluster itself is often an all-electronic display system simulating the traditional mechanical instruments and in time we expect the entire dashboard to become a single display surface
Powertrain: Under the hood of any modern vehicle there is always an Electronic Control Unit (ECU) for the engine and transmission utilising temperature, pressure, rotation and other sensors to control fuel injection and ignition timing according to the driver’s demand and making the most efficient use of fuel with minimisation of emissions. In the emerging electric vehicle or hybrid powertrains there will be next-generation ECUs for electric motor control and battery management.

Chassis: Almost all modern vehicles incorporate real-time electromechanical control and actuation systems for safer braking and electric power steering. Combined with traction control these provide for vehicle stability and legislation is in force which mandates that such features must be present in all modern cars.

Body electronics: This describes the many electronic systems around the vehicle, often providing for comfort and convenience and including motor control systems. Window lifters, adjustable mirrors, adjustable seats, heaters and air conditioners fall in this category. In addition the vehicle lighting system would be considered as part of the body electronics.

Driver assist: This category has only recently come into being and it describes an array of driver aids such as reversing cameras, parking sensors, cruise control etc. However, progress continues into the next category.

Advanced Driver Assistance Systems: ADAS is rapidly emerging as the next big innovation for automobile electronics. Usually employing video cameras or radar systems the electronics processes images in order to provide the driver with additional information and, in some cases, to automatically take some control of the vehicle powertrain or chassis. These systems require a large of amount of computation capability and amongst them are lane departure warnings, blind spot detection, parking assistance, dynamic cruise control and pre-crash braking.

Figure 1: ADAS Applications

In the modern vehicle, all of these systems are interconnected using a dedicated and robust communications network designed specifically for automotive such as CAN (Car Area Network), LIN, FlexRay or TTP (Time-Triggered Protocol). These busses have saved the industry millions and
contributed hugely to modern vehicle quality and reliability because they replace kilometres of electrical wiring harnesses.

The car area networks transfer data and control signals between the tens, if not hundreds, of ECUs hidden all around the car and the various sensors and actuators they control. Each ECU will have inside one or more microcontrollers containing an ARM processor, or some other kind of processor. And each ECU will contain a program memory with many kilobytes of software programmed into it.

Overall, the cost and complexity of automobile electronics is rapidly escalating as next generation powertrain, ADAS and other systems are introduced. Millions of lines of software source code will be brought together from many different sources into a single vehicle. The overall computation capability in any modern vehicle easily exceeds that which sent men to the moon. However, it is vitally important that automotive electronics system communications and interactions are carefully managed and segregated such that, for example, a fault in the IVI system cannot propagate into the chassis control. Consequently, automotive software development times can be protracted and delay new vehicle introductions. Software issues are also causing an increasingly significant number of breakdowns and recalls for upgrades.

![Automotive Electronics Complexity](image)

Figure 2: Automotive Electronics Complexity

Different kinds of microcontroller will coexist in the modern vehicle. Some will deliver very high performance to satisfy the requirements of ADAS image processing or IVI, whereas others will be dedicated to fast real-time control in the powertrain or chassis. Other kinds or communications network are also emerging such as in-car Ethernet and WiFi for passengers to use tablet computers and these can connect to the wide area using robust 4G wireless communications according to the latest LTE and LTE-Advanced standards. There is also increasing interest in the addition of telematics; a form of Machine-to-Machine (M2M) communications for monitoring service intervals, upgrading software and maintaining lifetime engagement between the customer and the vehicle manufacturer. And in the not too distant future we may see new kind of wireless communication between vehicles; so-called Vehicle-to-Vehicle (V2V), Vehicle-to-Infrastructure (V2I), both of which together are becoming known as V2X.
V2X Communications

V2V and V2I (i.e. V2X) communications between vehicles and roadside infrastructure is a rapidly emerging technology with huge potential to reduce to cost of traffic congestion, reduce the number of accidents and to save lives. V2X will use Dedicated Short Range Communications (DSRC) at 5.9 GHz for anonymous communication, i.e. the system is not intended to track individual vehicles or people but just to signal the presence of a vehicle and its status. Data transmitted from vehicles might include speed, direction and whether the vehicle is indicating to turn, accelerating or braking. (Elsewhere this technology is also referred to as a Wireless Access Vehicle Environment or WAVE.)

![Figure 3: V2X Communications](image)

V2X is not necessarily about autonomous driving or taking control away from the driver, it is positioned as the next logical step for ADAS with the capability to take account of surrounding vehicle movements. The potential is clear; using V2X communications could help prevent many accidents and save lives, for example by alerting drivers if they are about to pull out in front of an oncoming vehicle or drive into the back of a stationary vehicle around a blind bend or even about to encounter a major multi-vehicle collision when visibility is reduced on major highways. Interaction with roadside equipment could, for example, help to prevent drivers from crossing a red light or turning the wrong way and the roadside equipment could also relay data about what lies ahead and assist with congestion reduction.

Trials of V2X are under way right now in Europe and the USA where estimates by the Department of Transport show it has the potential to save over 200 billion dollars of annual cost to the US economy. This technology is rapidly gathering momentum with semiconductor devices for V2X communications.
being made available from innovative companies such as AutoTalks Ltd\textsuperscript{a} in Israel. Initial deployments are anticipated towards year 2020; no doubt legislation requiring it be fitted to all new vehicles will follow.

**ARM Processors for Automotive**

ARM processors are available today to support the majority of computation requirements in vehicles which offer the abovementioned features for drivers and passengers. A number of ARM Silicon Partners specialise in automotive devices, both catalogue microcontrollers and application-specific semiconductor products. ARM\textsuperscript{®} Cortex\textsuperscript{®}-A application processors are well established in the IVI space and are being designed into ADAS and other systems. ARM Cortex-M microcontroller processors are widely used in body control applications as well as in intelligent sensors for the engine and elsewhere. However, the most critical automotive applications require something extra as they must be reliable if they are controlling braking, steering and powertrain systems, and this is the domain of the ARM Cortex-R real time processors.

ARM Cortex-R processors\textsuperscript{iv} offer high performance whilst maintaining a deterministic response to hard real time events. The architecture of these processors, ARM Cortex-R4, ARM Cortex-R5 and ARM Cortex-R7, is specifically designed to allow the processor to respond to an event such as an interrupt from a mechanical sensor within a short period of time that is predictable and bounded. In addition these processors offer so-called ‘safety features’ with capability to manage faults occurring both in memories and in logic circuits, including the processor itself.

![Figure 4: The ARM Cortex-R5 Processor](image)

Fault management is a key attribute of many automotive systems. Faults in a semiconductor device can arise due to many causes including radiation, interference, device ageing and coding errors in the program. They are classified as either random faults which can appear at any time anywhere in the device or systematic faults which appear in a more consistent fashion, e.g. a software bug which always causes the same failure. Most random faults can be detected and perhaps corrected by including additional and normally redundant data and logic, i.e. Error Correction Codes (ECC) bits in memory and a
copy of the processor logic in a Dual Core Lock-Step system, or DCLS. These mechanisms are available for the ARM Cortex-R processors and can be utilised by designers for safety-related applications.

Both random and systematic faults are also managed by a Memory Protection Unit (MPU) within the ARM Cortex-R processor. The MPU can be programmed to prevent software from making an illegal access to selected regions of memory and peripheral address space. In case of an illegal access the MPU causes the processor to enter a special software routine which can manage the situation and possibly recover correct operation. This feature of ARM Cortex-R processors is defined within the ARMv7-R architecture as Protected Memory System Architecture, or PMSA.

**Functional Safety**

Automotive electronics controlling mechanical systems in a vehicle chassis such as braking, steering etc. are required to demonstrate a 'functional safety' capability, i.e. the active system should continue to function safely in the case of potentially hazardous events. This safety-related functionality can be achieved using techniques such as fault mitigation, e.g. detection and correction, or system-level management such as escalation to fail-safe operation. Overall the goal of functional safety is to assure freedom from unacceptable risk of injury or damage.

From an ARM processor perspective, functional safety requires inclusion of safety features within a processor or microcontroller device and their integration with other safety features in the product such as watchdog circuits and Built-In Self Test (BIST). Given the potentially hazardous consequences of failure in an automotive ECU, these safety features are of particular significance in automotive applications and also other fields of use such as factory automation and industrial control. With this in mind a new standard, ISO 26262, has been developed by the International Standards Organisation which defines functional safety for automotive applications throughout the lifecycle of all automotive electronic and electrical safety-related systems.

ISO 26262 has become increasingly significant as the automotive industry grapples with the increasing complexity and cost of automotive electronics and the hardware/software supply chain. The standard sets out best practise for functional safety product development processes and measurable risk management using an Automotive Safety Integrity Level (ASIL) ranging from A to D. Complexity is managed by standardising an approach for treating each component or sub-assembly in isolation as a so-called ‘Safety Element out of Context' or SEooC with both qualitative and quantitative data being provided for each SEooC. This approach enables the formal safety treatment of ARM’s processor core Intellectual Property (IP) within the automotive supply chain as it can be considered as a SEooC for use by a Silicon Partner putting it in the context of its semiconductor device.

The ARM Cortex-R5 and other ARM processors are being supported with additional data and documents necessary for ARM’s Silicon Partners to apply them in devices for safety-related applications. In particular, these documents and data describe the operation and effectiveness of the processor’s safety features for use by safety managers and engineers applying the IP as a SEooC within their product. This enables selected ARM processors to be used in safety-related applications according to standards such as ISO 26262 for automotive and IEC 61508 for general industrial use.
ARM’s initiative to support application of its processor IP in safety-related applications is key to the application of ARM technology in the increasingly complex automotive industry, both within vehicles and also in roadside infrastructure. The processing capability to support emerging applications such as ADAS and V2X is highly sophisticated and will employ many ARM Cortex-M, Cortex-R and Cortex-A processors in the various sensing, actuation and computation systems for automotive and highway infrastructure. Other established attributes of ARM technology such as energy efficiency, scalability, ecosystem support and security all make ARM-powered solutions an attractive choice for automotive engineers.

**ARM’s New Architecture: ARMv8-R**

With the forgoing in mind, ARM has developed a new Cortex processor architecture for real-time control and safety-related applications. Identified as ARMv8-R, technical details of this new architecture were first disclosed at the 2013 ARM TechCon conference. This new real-time architecture is for 32-bit processors and it builds on the ARMv7-R architecture as implemented in the Cortex-R5 processor with enhancements from the ARMv8-A applications architecture implemented in the Cortex-A53 and Cortex-A57 processors. ARMv8-R incorporates further key features to support processing for next generation automotive, highway and industrial applications including a Hypervisor mode, the ability to host both PMSA and VMSA operating systems and a new programming model for fast context switching. For convenience the key features of the ARMv8-R architecture are summarised here:

**Hypervisor:** Introduction of an additional level of privilege (Privilege Level 2 or PL2) into the processor hardware supporting a Virtual Machine Monitor which can handle interrupts and events with real time determinism whilst supporting and switching between multiple Guest Operating Systems running normally at PL1. This ‘bare metal’ support enables very fast context switching from a Guest OS into a real time device driver’s interrupt handler, or into another Guest OS context.

**PMSA/VMSA support:** PMSA, or Protected Memory System Architecture, is supported as standard in Cortex-R processors and is always used at PL2. However, a Guest OS running at PL1 may instead employ VMSA, or Virtual Memory System Architecture, with accompanying Memory Management Hardware (MMU) in the processor. Thus an ARMv8-R processor could run a ‘rich’ OS such as Linux or Green Hills System’s Integrity OS whilst being able to respond deterministically to hard real time interrupts by entering either the Hypervisor mode or another virtual machine context. Applications or real time tasks will normally run at PL0. Note that the Hypervisor mode does not support a second level of virtual memory management and programs running at PL2 or in a real time context are therefore not subject to delays caused by a virtual memory system performing a page table walk.

**Memory Protection:** Two stages of memory protection are provided in ARMv8-R. Stage-1 is managed by programs running at PL1 and therefore controlled by the Guest OS. Stage-2 is exclusively controlled from Hypervisor mode PL2 and can therefore provide for isolation between Guest OSs and their tasks or applications. This isolation, or ‘sandboxing’, allows software from different sources or for different safety-related applications to be consolidated onto a single processing platform in the knowledge that any unwanted access to regions of the address map for memory and peripheral devices can be prevented. Moreover, the ARMv8-R architecture
specifies a new programming model for the Memory Protection Unit (MPU) facilitating much simpler and faster programming of address regions and their attributes.

Figure 5: ARMv8-R Privilege Levels

When combined with other safety features implemented in ARM Cortex-R processors, the ARMv8-R architecture enables a new and unrivalled capability in automotive electronics which permits consolidation of multiple tasks and applications onto a single energy-efficient processor. This should fulfil the emerging requirements of applications such as ADAS and V2X where high level, but less reliable, information is processed before actuating chassis and powertrain systems in real time.

ARMv8-R architecture is the enabling technology for the next generation of ARM Cortex-R processors to be used within new automotive microcontrollers and application-specific semiconductor products. The features in ARMv8-R will make system complexity and functional safety more manageable and reduce overall cost in the automotive industry. Software portability and reuse should be increased and software from different sources can coexist on the same ECU. Overall ARMv8-R is expected to make a positive contribution to automotive electronics quality and reliability.
Conclusion

ARM has announced its new ARMv8-R architecture at the 2013 ARM TechCon conference; however, ARM has not released any details of processor IP products implementing the new architecture at this time. The intent of the architecture announcement is to enable early development of the ecosystem around ARMv8-R, in particular for those companies working on Operating Systems for safety-related applications such as the AUTOSAR community. Through this announcement, ARM is also providing visibility for tier-one suppliers and OEMs in the automotive and industrial sectors where long-term product planning is the norm and wider awareness can usefully be promoted.

About the Author

Chris Turner is responsible for marketing of the Cortex-R series processors at ARM in Cambridge UK. Chris has a wealth of experience in communications, computing and semiconductors with previous career positions at Cambridge Consultants, Virata Corp, Olivetti Research, Acorn Computers and Philips. At ARM, Chris focuses on applications for high performance, real-time embedded processors, including dependable systems for automotive, high performance storage and the evolution of 4G mobile baseband. Chris is a Chartered Engineer, registered European Engineer (Eur Ing) and an IET Fellow.
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