ARM®

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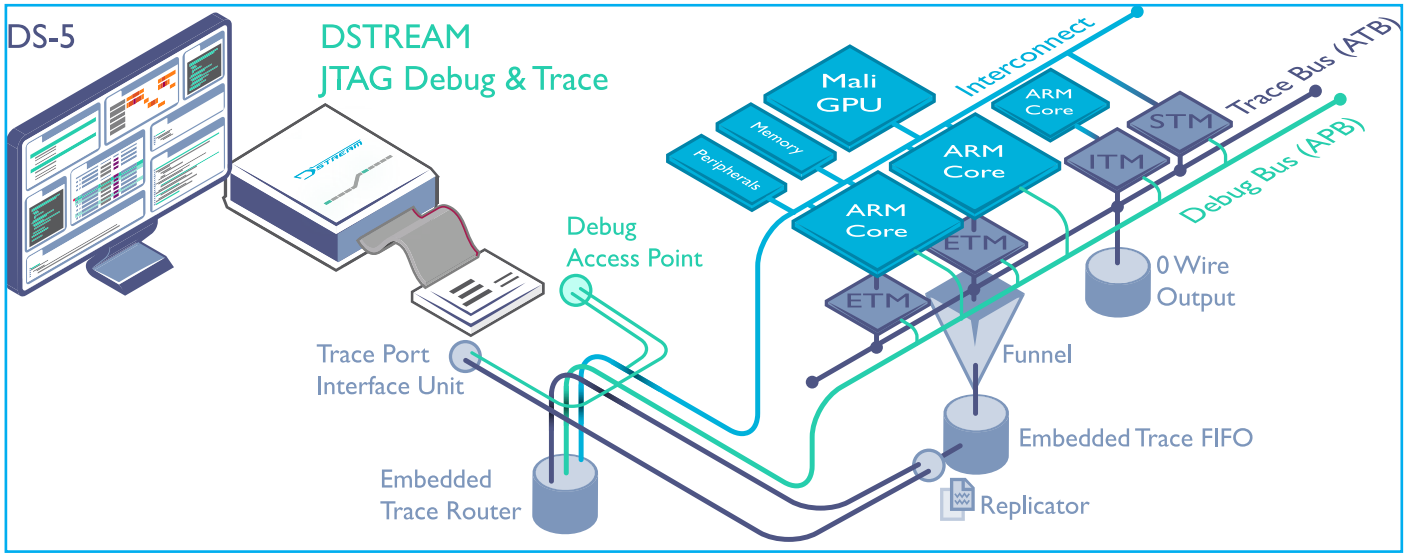
ARM® CoreSight™
Building Optimized ARM SoCs

Modern SoCs are continually increasing in complexity and packing in more and more features. Large designs with multiple CPU architectures, GPUs, numerous power domains, various DVFS regions, big.LITTLE™ and advanced security schemes are very common. This in turn adds a big overhead for silicon bring-up and software development/optimization while at the same time designers are under pressure to keep costs down.

CoreSight, ARM's debug and trace product family, is the most complete on-chip debug and trace solution for the entire System-On-Chip (SoC), making ARM-based SoCs the easiest to debug and optimize.

Key Benefits

- Higher visibility of complete system operation through fewer pins
- Standard solution across all silicon vendors for widest tools support
- Re-usable for single ARM core, multi-core or core and DSP systems
- Enables faster time-to-market for more reliable and higher performance products
- Supports for high performance, low power SoCs



CoreSight DAP

The CoreSight Debug Access Port provides software debugger access to the debug and trace subsystem within a SoC. The DAP supports access through JTAG or, for pin limited applications, Serial Wire Debug (SWD) offers the same functionality over two pins.

CoreSight STM

The CoreSight System Trace Macrocell enables low latency and high bandwidth *printf* style debug capability that gives developers more visibility into their software without altering the system behavior, making it easier to develop and optimize software on ARM processor-based systems.

CoreSight TMC

The CoreSight Trace Memory Controller (TMC) provides a range of trace collection solutions to manage and deliver real-time trace in a cost effective manner during all product development phases' right up to final products. TMC introduces a new FIFO mode enabling averaging of trace over a long period, reducing risks of overflows and allowing smaller trace port.

ARM® CORESIGHT™

Processor Debug & Trace IP

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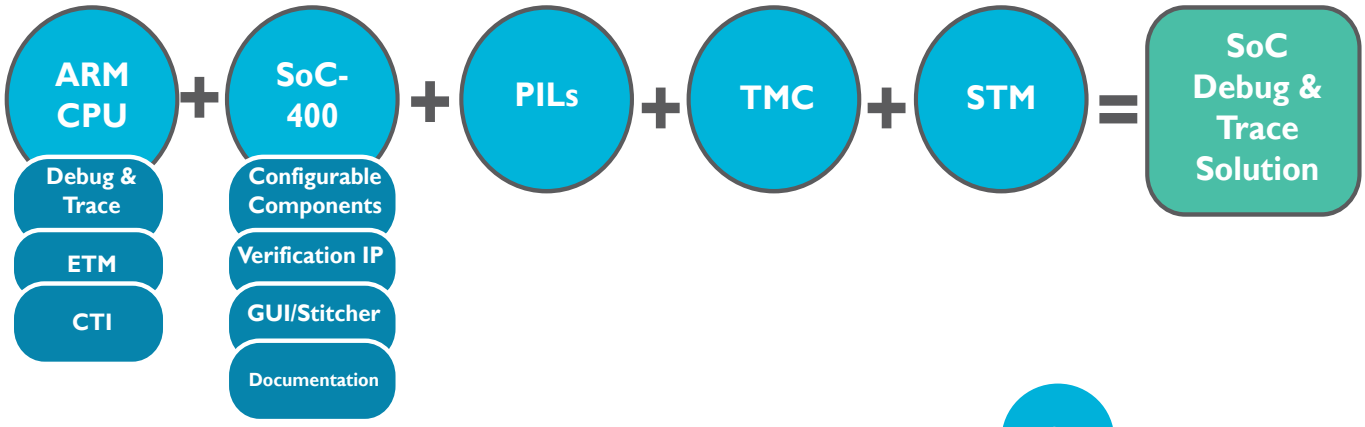
CoreSight SoC-400

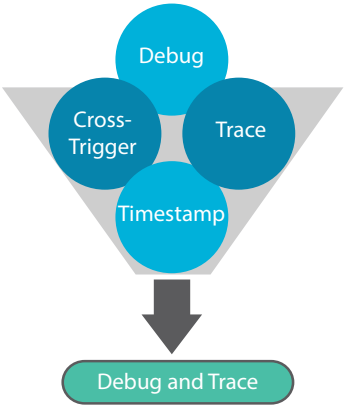
The CoreSight SoC-400 provides a kit of parts to build and validate a debug a trace subsystem within an SoC design. These components, in conjunction with the CoreSight Trace macrocells, provide the whole infrastructure required to debug, monitor, and optimise the performance of a complete System on Chip (SoC) design. CoreSight SoC-400 has been designed to address the high bandwidth requirements of multi-core debug and trace and to provide access to whole systems beyond the core.



CoreSight Timestamping and Cross Triggering

CoreSight supports the generation and distribution of 64 bit timestamps, enabling time correlation of multiple debug and trace sources across a SoC

CoreSight also offers cross-triggering capabilities for distribution of trigger events, thus enabling a SoC component to control the actions of other components.



Debug Tools Support

For the debug and trace solution to be effective, it is critical to have advanced debug tools support. ARM has defined an open CoreSight architecture to allow SoC designers to add debug and trace capabilities for other IP cores in to the CoreSight infrastructure. Therefore, this allows for widespread tool support in the ecosystem. The CoreSight technology is supported by over 25 industry-leading software and hardware debug tools companies across all markets and regions.

ARM DS Development Tools

ARM KEIL Microcontroller Tools

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CoreSight Debug and Trace

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Web: j.mp/CoreSight

Call us

UK
T: +44 1223 400400

JAPAN
T: +81 45 477 5260

CHINA
T: + 8621-6154 9000

USA
T: +1 408 576 1500

SOUTH KOREA
T: +82 31 712 8234

INDIA
T: +91 80 4928 2000

GERMANY
T: +49 89 456040 20

TAIWAN
T: +886 2 8751 1717

FRANCE
T: +33 1 39 30 47 89