Leveraging Advanced Physical IP to Deliver Optimized SoC Implementations at 40nm and below

John Heinlein, Ph.D.
Vice President Marketing
ARM Physical IP Division
November 19, 2010
Consumer Driving Decade of Change
Connectivity Driving The Future

1st Era
- Mainframe
  - 1MM+ Units
  - 1960

2nd Era
- Minicomputer
  - 10MM+ Units
  - 1970
- Desktop Internet
  - 1B+ Units/Users
  - 1980

3rd Era
- Mobile Internet
  - 10B+ Units?
  - 1990
- The Internet of things
  - 100B+ Units
  - 2000
- 2010
- 2020

Increasing Connectivity
Convergence Driving SoC Requirements

Software stack optimized for Cortex™ + Mali™

Comprehensive range of video standards on NEON™ and Mali-VE

Tools support for CoreSight™

Coherency and virtualization

Secure systems on TrustZone®

ARM Compute Subsystem

Graphics processor

Video

Foundation IP & POPs

Interconnect & memory controllers

MobiCore
Integration Complexity & Specifications

- 1 GHz or more
- 0.5 mW per MHz
- 1 mW standby power
- 400 MHz or more
- HD memory banks

**ARM Compute Subsystem**

- **Graphics processor**
- **Video**

**Foundation IP & POPs**

- Interconnect & memory controllers
- MBIST Support
- Software compatibility

- DFI 2.0 Compliant
- Data Rates > 1600 Mbps
Outline: Addressing SoC Challenges

- Innovation in ARM Artisan physical IP

- Advanced Process Technologies

- Co-developed optimizations for cores

- Bringing advanced technology to older geometries
ARM Offers Broadest Foundry Solution

- Extensive Process Optimized IP Portfolio

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designstart.arm.com
Fully Independent Physical IP Provider

Artisan®
Advanced Physical IP by ARM

ARM Physical IP
Logic
Memory
GPIO
DDR

Apache Design Solutions
Cadence
Magma
Mentor Graphics
Synopsys

Samsung
IBM
GLOBALFOUNDRIES
SMIC
UMC
Dongbu
Tower Semiconductor
SilTerra

The Architecture for the Digital World®
Artisan Physical IP: Technical Leadership
ARM Leading **Multi-channel** Libraries

- ARM multi-channel length advantages include:
  - **Finer grained tradeoffs** between performance and leakage reduction
  - **Better low voltage operation** as long channel device RVT performance degrades less with lower voltages than HVT device
  - **Lower cost** because multi channels require no additional mask layers

- ARM footprint compatible MC libraries work:
  - With **standard synthesis and place & route** tools
  - Without the need for any **additional design** steps
Benefits of Multi-channel Libraries

- Provides larger leakage/performance spread
- Fine resolution for design trade-offs
New Market-leading Memory Products

- New in 2010: Fundamental memory compiler redesign
- Project Goals
  - Deliver market leading PPA (Power, Performance and Area)
  - Develop modular development methodology to speed time to market
- Deploying now at 65nm, 55nm, 40nm and 28nm nodes

- Example: Planned SMIC 40LL high density compilers superior area

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<tr>
<th>Compiler</th>
<th>Instance</th>
<th>Vendor</th>
<th>Best area (sq µm)</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>High density single port</td>
<td>8192x16</td>
<td>ARM</td>
<td>49600</td>
<td>✓ ARM 21% smaller</td>
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<tr>
<td></td>
<td></td>
<td>Competitor</td>
<td>62600</td>
<td></td>
</tr>
<tr>
<td>High density single port</td>
<td>2048x16</td>
<td>ARM</td>
<td>14200</td>
<td>✓ ARM 17% smaller</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Competitor</td>
<td>17100</td>
<td></td>
</tr>
<tr>
<td>High density two port</td>
<td>32x34</td>
<td>ARM</td>
<td>3000</td>
<td>✓ ARM 33% smaller</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Competitor</td>
<td>4500</td>
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</table>
Physical IP New Feature Timeline

2011-2012
- Variation tolerant: High performance & low power yield improvement technology

2010
- Streamlined high density and low Vdd memory compilers
- Dual row programmable fail safe GPIOs
- Lithography-aware layout
- Processor optimization packs launch

2009
- First commercially available multi-channel libraries

2008
- Extended memory test features

2006
- DFM-aware layout
- Power format support (UPF/CPF)

2005
- Integrated memory power management
Advanced Process Technologies
ARM 32/28nm Platform

28nm Platform
- Logic
- Memory
- GPIO
- DDR

“G” Platform
- 28HP
- 32LP
- 28HPP

“LP” Platform
- 28HPL
- 28LP
- 28SLP
Common Platform 28nm LP Platform

Comprehensive 28LP Physical IP platform

- Rich foundry-sponsored foundation IP
- End-user licensable enhanced IP
- Multi-channel logic products for 9 and 12 track
- Market-leading memory compilers:
  - Write Assist, Mixed Vt, flexible power gating
  - Low voltage operation

Processor Optimization Pack for Cortex-A9

- Targets >1 GHz Cortex-A9 (worst case)

Product Availability and Silicon Validation

- IP available in Q4 2010
- Test chip tape out Q4 2010
Requires Major Commit to Si Validation

- Validated ARM Physical IP and integrated SoC design flow
- Broad range of experimentation needed for proven success:
  - Early chips to decide architecture choices
  - Silicon validation to ensure IP quality
  - Prototype implementation for proven power / performance / area achievement
ARM TSMC 28nm HP Platform

**Comprehensive 28nm Physical IP platform**
- End-user licensable enhanced IP
- Multi-channel logic products for 9 and 12 track
- New architecture memory compilers:
  - Mixed Vt, mixed channel length, flexible power gating

**Processor Optimization Pack for Cortex-A9**
- > 2GHz target for Cortex-A9 in development

**Product Availability**
- Evaluation libraries available Now
- Alpha libraries in Q4 2010
- EAC production release in Q2 2011
- Testchip tape out in Q1 and Q2 2011

**Logic**
- 2 Libraries, Multi-Vt/Channel
- Power Mgmt, ECO

**Memory**
- 6 Memory Compilers

**IO**
- DDR2/3

**Processor Optimization**
- Cortex-A9 Optimizations
ARM Platform for TSMC 40LP Process

Comprehensive Physical IP Platform

- Multi-channel logic products for 9 and 12 track
- New architecture memory compilers:
  - New low leakage mode
  - Embedded scan chains for DFT
  - Long channel usage reduce mask cost

Logic
- 9 and 12 track standard cells, Multi-Vt and Multi-channel
  - Power Mgmt, ECO

Memory
- 5 Memory Compilers

Performance Optimization Package for Cortex-A9 and Cortex-A5

- Targeting 1GHz Cortex-A9 available JAN-2011
- 600+ MHz target for Cortex-A5 in development

Processor Optimization
- A9 Optimized IP
- A5 Optimized IP

Product Availability and Silicon Validation

- IP available – NOW (Production PDK)-
- Test chip tape out Sept 2009
- Test chip report – Jan 2011

Interface
- DDR 3/2 PHY
- GPIO 2V5 Gox (In Dev)
Processor Optimization Packs

ARM Artisan
Processor Optimization Pack “POP”

Optimize for performance or power
Comprehensive implementation solution
Silicon proven results
Fast time to market

Achieve up to 25% increase in performance or more than 80% reduction in leakage power

Cortex-A9
Optimized Physical IP

ARM Benchmarking
Implementation Knowledge
Where Do the Gains Come From?

- Example: TSMC 40nmG improvements vs. baseline

- Percentage of overall performance improvement by technique:
  - Physical IP: 45%
  - Floorplan: 25%
  - Flow: 19%
  - RTL: 11%
Physical IP Optimizations: L1 Memories

1. Low profile feature set
2. IO Tuned to Processor requirements
3. Architectural range optimized for L1 cache sizes & performance
4. IO Scan Chain (increased testability/ reduced pattern count)
5. Power Efficiency Options
   - GL Bitcell Option

+ Instance based characterisation for variety of operating conditions
Physical IP Optimizations: Logic

- High Performance Macro: targeting 2GHz (LVt, OD)
  - 40nm base libraries very, including complex cells / varying drive strengths (over 1000 cells)

- Supplemental “High Performance Kit”
  - Base 12-track library strain optimized for performance
  - Tapered cells added to library
  - Increase drive strength / beta ratio of cells for better stage gain
  - Optimized FF’s (CLK→Q, small setup)
  - Additional AOI / OAI functions

- Result: 60%+ hit rate on critical paths, resulting in additional 80MHz frequency
ARM announces processor optimization packs for ARM Cortex-A9

ARM delivers optimized Artisan physical IP enabling SoC designers to achieve up to 1.7 GHz performance on TSMC 40nm G process in worst case conditions

Cambridge, UK – November 9, 2010 – ARM today announced the immediate availability of the ARM® Cortex™-A9 Processor Optimization Packs (“POPs”). Processor Optimization Packs leverage ARM Artisan® physical IP to enable customers to achieve technology leading performance or power targets on their Cortex-A9 implementations in the shortest time to market. A silicon-proven POP is available now TSMC 40nm G process technology. The Cortex-A9 POP on TSMC 40nm LP process technology will be available to customers in January 2011.
Cortex-A9 TSMC 40G – Speed Optimized

Performance Optimized

2GHz
Typical Silicon

1.71GHz
OD, <3% LVt

1.29GHz
RVt

Implementation with Enhanced IP
- High performance kit
- Multi-channel libraries
- Fast cache instances
- High speed standard cell architectures

950MHz
RVt

Implementation with Enhanced IP
- Multi-channel libraries
- Multi-Vt
- High speed memories

850MHz
(out of the box)

Implementation with Foundation IP

-worst case conditions; SS, 0.81V, 125C (Nominal); SS, 1.0V, 105C (Overdrive)

ARM Developed
Hard Macro

Implementation using
Cortex-A9
Performance Optimization Pack

Implementation with standard physical IP

Partner Licensed Macro
Partner Licensed IP
Foundation IP

Foundry Funded IP

Foundation IP

Partner Licensed Macro
Partner Licensed IP
Foundation IP

The Architecture for the Digital World®
Cortex-A9 TSMC 40G – Power Optimized

<table>
<thead>
<tr>
<th>Power Improvement</th>
<th>Silicon Devices</th>
<th>Hard Macro Implementation</th>
<th>Implementation with Enhanced IP</th>
<th>Implementation with Foundation IP</th>
</tr>
</thead>
<tbody>
<tr>
<td>5mW</td>
<td>Power shut-off</td>
<td>ARM Developed Hard Macro</td>
<td>Implementation using Enhanced IP</td>
<td>Implementation with Foundation IP</td>
</tr>
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<td></td>
<td>using PMK</td>
<td></td>
<td>- High performance kit</td>
<td>- All worst case conditions; SS, 0.81V, 125C</td>
</tr>
<tr>
<td>0.66W</td>
<td>50nm MC, RVT/HVT</td>
<td></td>
<td>- Multi-channel libraries</td>
<td></td>
</tr>
<tr>
<td>1.15W</td>
<td>50nm MC, RVT/HVT</td>
<td></td>
<td>- Fast cache instances</td>
<td></td>
</tr>
<tr>
<td>1.25W</td>
<td>50nm MC, RVT</td>
<td></td>
<td>- High speed standard cell architectures</td>
<td></td>
</tr>
<tr>
<td>3.83W</td>
<td>40nm MC, RVT</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.96W</td>
<td>RVT</td>
<td></td>
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800 MHz Speed

ARM Developed Hard Macro

Implementation using Cortex-A9 Performance Optimization Pack

Implementation with standard physical IP

Partner Licensed Macro

Partner Licensed IP

Foundation IP
**Cortex-A9 TSMC 40LP – Speed Optimized**

- **1.15 GHz** (Typical Silicon)
  - Implementation with Enhanced IP
    - High performance kit
    - Multi-channel libraries
    - Fast cache instances
    - High speed standard cell architectures

- **1.0 GHz** LVt & OD
  - Implementation with Enhanced IP

- **0.85 GHz** Mixed Vt
  - Implementation with Enhanced IP
    - Multi-channel libraries
    - Multi-Vt
    - High speed memories

- **0.78 GHz** RVT
  - Implementation with Enhanced IP

- **0.6 GHz**
  - Implementation with Enhanced IP

- **0.5 GHz** (out of the box)
  - Implementation with Foundation IP

- All worst case conditions; SS, 1.08/0.99V, 125C

**Partner Licensed IP**

**Foundation IP**
ARM ANNOUNCES 32NM CORTEX-A9 OPTIMIZATIONS

World’s first 32nm Cortex™-A9 core test chip implemented on Samsung HKMG process using ARM Processor Optimization Pack

Santa Clara, CA – November 9, 2010 – ARM today announced their newest optimization package for the ARM® Cortex™-A9 processor, targeting Samsung 32nm LP High-K Metal Gate (HKMG) process technology. This ARM Processor Optimization Pack (POP) provides a highly tuned foundation for implementing Cortex-A9 processors in low power, mobile applications. Based on ARM Artisan® optimized logic and memory physical IP, the POP is also supported by implementation knowledge and ARM benchmarking, providing a rich foundation for leading edge System-on-Chip (SoC) designs. The Processor Optimization Pack enables operation over 1 GHz, and is available for immediate licensing from ARM.
Cortex-A9 Samsung 32LP – Speed Optimized

1.47GHz typical

1.24GHz
10% LVt, OD

Implementation with Enhanced IP
- SC12MC LVT C30 Base Library
- SC12MC LVT C30 HPK
- SC12MC RVT C30 HPK
- L1 Fast Cache Instances RVT

1.08GHz
10% LVt

Implementation with Enhanced IP
- SC12MC RVT C30 HPK
- L1 Fast Cache Instances RVT

980MHz RVT

Implementation with Enhanced IP
- SC12MC RVT C30 HPK
- L1 Fast Cache Instances RVT

795MHz (out of the box)

Implementation with Foundation IP
- SC12MC RVT C30 Base Library
- L1 instance from memory compiler SP-RF-HS

- All worst case conditions; SS, 1.045/0.95V, -40C

Partner Licensed IP
Foundry Funded IP

Implementation using Cortex-A9 Performance Optimization Pack

Implementation with Standard Physical IP
32nm Cortex-A9 Silicon Results

- Speed-optimized ARM Cortex-A9 achieves 1.24 GHz on low power process.
- Silicon proof-point of Common Platform 32nm low power (LP) High-K Metal Gate (HKMG) process technology.
Breadth of Portfolio

ARM Artisan Foundation IP
ARM Offers Broadest Foundry Solution

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New IP in 2010
Existing platforms

designstart.arm.com
Physical IP for Embedded Processors

**Ultra Low Power**
- TSMC CV011LP
- TSMC CM011LP
- TSMC CL011LVP
- TSMC CE018FG
- GF 180ULL

- Leakage-optimized
- Ultra high density standard cells
- Ultra low power memories
- Low power I/Os

**Mainstream**
- Tower 110G
- TSMC CM011G_Hybrid
- Grace 180G
- TSMC 180G

- Area-optimized
- Ultra high density standard cells
- High density memories

**High Performance**
- GF 110G
- SMIC Logic011
- TSMC CL011G

- Performance optimized
- High density standard cells
- High speed memories
Thank you!