Growth in mobile computing and the Internet of Things is connecting more devices and aggregating more data across the network, and that demands an increasingly flexible and efficient computing infrastructure. The CoreLink CCN family offer the solution with scalable, high performance cache coherency for ARM Cortex® processors, memory and IO such as accelerators and network interfaces. The CoreLink CCN interconnects are designed for the latest AMBA® 5 CHI protocol providing high frequency, non-blocking data transfers and integrated Level 3 Cache and Snoop Filter.

**Cache coherency across processors, IO and accelerators**

The CoreLink CCN-512, CCN-508, CCN-504, CCN-502 and CCI-400 interconnects provide a spectrum of implementations scaling from cost-efficient, minimal area, single core systems, up to the highest performance 48 core systems. All of the CCN family offer a common architecture with integrated configurable L3 cache which can operate as a system cache allowing allocation of IO traffic. The CoreLink CCN family and companion CoreLink DMC-520 Dynamic Memory Controller are designed for high reliability with integrated RAS and ECC features to protect data. Advanced end to end Quality-of-Service (QoS) mechanisms enable the control required for maximum bandwidth and minimum latency.

CoreLink CCN-502 is the most cost- and power-efficient solution in the CCN family offering 70% area reduction over CoreLink CCN-504 at 1MB. Applications may include small cell base stations and sub-10W Power-over-Ethernet wireless access points. CoreLink CCN-512 offers the highest compute density, scaling up to 12 cluster, 48 core, 64-bit ARMv8-A, systems. Applications may include macro cell base stations, data center and servers.
Extending the ARM CoreLink Cache Coherent Network Family

The CoreLink CCN-502 and CCN-512 are the newest members of the Cache Coherent Network family.

CoreLink CCN-502
High Performance, Small Footprint

Key Features of the CCN Family:
- Scalable architecture offering software compatibility
- Native AMBA CHI interfaces providing high frequency, non-blocking data transfers
- End-to-end QoS and RAS

- Integrated Level 3 Cache and Snoop Filter
- Designed for the 64-bit ARMv8-A processors including Cortex-A57 and Cortex-A53
- Part of complete solution including Cortex processors, CoreLink DMC-520 Dynamic Memory Controller, CoreLink MMU-500 System MMU and CoreLink GIC-500 Interrupt Controller.

CoreLink CCN-512
Maximize Compute Density

www.arm.com/products/system-ip/interconnect

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