ARMv8-Based SoC HW/SW Integration and Verification Solution

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Example ARM®-based HW/SW System
Challenges at the SoC, System, & SW level

Multi-core early software bring-up and integration on 64-bit

Developing environments for hardware/software integration and use-case verification on simulation/emulation platforms

Bare-metal software use-case testing to verify multi-core cache and I/O coherency, concurrency, power shut off, etc...

Verification of IPs on AMBA interconnect with adherence to ACE protocol

Debugging of complex multi-core SoC software scenarios on RTL simulation/emulation platforms

Characterizing and analyzing system-on-chip (SoC) performance and efficiently debugging issues

How do I represent the SoC environment?
Accelerating ARM-based development
Early OS & Software Bring-up
Accelerating ARM-based development
Early SW Execution on Palladium

TLM Virtual Platform – VSP
- Up to 100MHz
- Early Availability for SW Developers
- Advanced SW Debug
- Fast SW Turnaround Time

Emulation – Palladium® XPI/II
- Up to 4MHz
- From early-RTL to full-SoC Validation
- Advanced HW Debug
- Fast HW Turnaround Time

Hybrid Solution with SW Integrator
- Boot Complex OS at 48MHz
- Speed UP SW-Driven tests 1-10X over emulation
- Early Availability for SW Developers
- Advanced HW + SW Debug
- Fast HW and SW Turnaround Time
Palladium/VSP Hybrid Solution

**Architected for SW Performance**
- High-speed virtual platform
- Asynchronous HW/SW Execution with Interrupt driven sync
- High-Speed Multi-Domain Memory Coherency

**Designed to integrate HW and SW flows**
- Does not require changes to HW or SW stacks
- Virtual connections into SW Engineer’s environments
- Seamless hybrid execution for both HW and SW users

**Proven Methodology, Unique Expertise**
- Cross-platform and design integration expertise
- Exclusive hybrid methodology delivers performance and repeatability
- Proven during successful application to SW-rich SoCs
Hybrid Example

Execute SW at 100MHz
With standard or custom processor models

Plug and Play Integration with RTL
SoC-specific transactors and RTL I/F

Validate SoC + OS at 5-10 MHz on PXP
High-performance memory coherency

Shorten SoC Debug
System Messages
HW / SW Debuggers
NVIDIA Example: Performance Results

- Boot OSes, run real world applications and benchmarks
  - Linux kernel boot
    - Palladium only = 45 mins
    - Hybrid = 2 mins
  - Android
    - Palladium only = Hours*
    - Hybrid = 40 - 50 mins
  - Windows
    - Palladium only = Days*
    - Hybrid = 75 - 90 mins

Source: System to Silicon Verification Summit 2013
http://bit.ly/1cT4py2
Performance Analysis
Performance Analysis
ARM ARMv8-A mobile example SoC
ARM ARMv8-A mobile example SoC

Performance challenges

What is the latency of the processor clusters to memory paths including all async bridges?
ARM ARMv8-A mobile example SoC
Performance challenges

What is the latency of the processor clusters to memory paths including all async bridges?

What is the bandwidth of the paths from IP with high bandwidth demands to memory?
What is the bandwidth and latency of the paths from real-time IP to memory?
Interconnect Workbench

For Interconnect IP Integration
• Performance of use-case traffic loads
• Verify configuration functionality

For SoC Integration
• Validate performance in context of IPs

Benefits
- Shorten performance tuning and analysis iteration loop from days to hours
- Reduce testbench development time from weeks to hours
Component interconnect testbench – Functional verification

Using ARM® AMBA® Designer IP-XACT
Subsystem testbench

Using IP-XACT or CSV metadata
Analyze performance results

Charts split by burst length

Increasing bandwidth as burst length increases
Significant challenges in predicting and optimizing SoC performance
  - Multiplicity of IP configuration options particularly in interconnect and DDR space
  - Need a systematic approach with the potential to be automated

Performance verification accomplished in three steps
  - Characterization: Fully automated and can be checked as a standard regressions step
  - Architectural: Establish QoS functions as expected
  - Use case: Hunt for corner case issues

Cadence® Interconnect Workbench supports all stages of the process
  - Automation of testbench, supports ARM CoreLink® System IP
  - Automation of the characterization tests
  - Comprehensive analysis and checking capabilities
  - Traffic synthesizers for architectural and use-case analysis
HW/SW Debug
HW/SW Debug

- Cadence® Palladium Hybrid solution for early OS and SW Bring-up with ARM® Fast Models and ARM DS-5 Development Studio
  - Software Debug: C Code

- Cadence Incisive® Debug Analyzer Synchronized Embedded SW Debug on ARM RTL CPU
  - Hardware Debug: RTL

- Cadence Verification IP for ARM AMBA and other interface protocols as well as memory models, with support on Incisive Formal Verifier, Incisive Enterprise Simulator, Palladium Acceleration

- ARM Cortex®-A, Cortex-M, Cortex-R Fast Models

- Cadence Interconnect Workbench for performance analysis and verification of ARM Corelink™ Interconnect based systems, including integration to ARM AMBA® Designer

- System Debug - Hardware
ARMv8-based SoC hardware/software debug solutions

Cortex®-A53/-A57 post-process SoC debug
- Integrated and synchronized hardware/software debug with testbench
- For verification and design teams
- Enables off-line debugging
- Consistent across IES and PXP

Cortex-A53/-A57 JTAG software debugger
- Interactive software debugging on PXP
- Support for software developers using RealView, Lauterbach, etc..

Synchronized with design and testbench debugger

Embedded C source code debug with assembly view

Software variable tracing
ARMv8-based SoC hardware/software debug solutions

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JTAG debugger support for software developers on PXP

ARM RealView Debugger

Lauterbach Debugger
Verification IP
ARM-related Verification IP

- ARM Cortex®-A, Cortex-M, Cortex-R Fast Models
- Cadence Interconnect Workbench for performance analysis and verification of ARM CoreLink™ Interconnect based systems, including integration to ARM AMBA® Designer
- High Speed, Wired Interface Peripherals
- General-Purpose Peripherals
- Low-Speed Peripherals

- Applications
- Middleware
- Operating Systems (OS)
- Drivers
- Firmware / HAL

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Cadence VIP for ARM AMBA specifications

• **Benefits**
  – Get to market first with latest I/Fs
  – Verifies SoC data integrity
  – Simplify protocol compliance
  – Maximize team productivity

• **Highlights**
  – #1 ACE VIP (ARM collaboration)
  – Coherent interconnect validation
  – Advanced compliance testing
  – Formal and acceleration support

• **Specification Support**
  – ARM AMBA CHI, ACE
  – ARM AMBA AXI4, AXI3
  – ARM AMBA AHB, APB

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**Maturity Level**

- 1-20 projects
- 20-100 projects
- 100-500 projects
- 500+ projects

**Compliance Method**

- Puresuite
- CMS
- TripleCheck

**Verification Technologies**

- Protocol Checks
- Trace Debug
- PureView Configurator
- Formal Analysis
- Interconnect Validation
- Acceleration Support

1 Accelerated VIP sold separately
Cadence cache-coherent VIP for ACE
Full set of VIP agents to verify cache coherent designs

- Generates coherent stimuli and responds to snoop bursts
- Includes cache model
- Can be configured as ACE or ACE-lite

- Monitors protocol correctness
- Collects coverage
- Includes cache model
- Can be configured as ACE or ACE-lite

Legend:
- DUT
- VIP

- Responds to read/write transactions
- Model sparse memory
- ACE-lite port

- Checks protocol correctness
- Collects coverage
- ACE-lite
Summary
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