Advanced Implementation of ARM® Cortex®-A57 / Cortex-A53 CPUs and ARM Mali™ GPUs in TSMC 16nm FinFET Process

ARM Tech Symposia
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Today's Markets and Design Focus

**Consumer**
- >90nm
- 65nm
- 40nm
- 28nm

**Mobile/Tablet**
- 28nm
- 20nm
- 16nm

**Enterprise**
- 28nm
- 20nm
- 16nm
Implementation Targets

- High Performance Mobile Cluster (big)
- Low-Power Cluster (LITTLE)
- Low-Power Server

Cortex-A57 MP4 + ECC, Fmax
Cortex-A57MP2/4, Fmax
Cortex-A53 MP4, Low-Power
Cortex-A53 MP4+ECC, Fmax
Being Late to Market Costs $$$

- Development cycle for mobile SoCs are at least 6-8 months
- Typical life-cycle of mobile SoC is 12-18 months
  - Maximum value is in the initial stages
- Any delay in launching the SoC seriously impacts profitability
  - Loss of revenue due to product delay
  - Opportunity cost due to impact to subsequent products

http://blackswanfarming.com/urgency-profiles/
International business strategies
Comprehensive Platform for TSMC 16FFLL+ FinFET Process

Products

- Standard Cell Libraries
  - High Performance
  - High Density
  - Ultra High Density

- Memory Compiler
  - Single, Dual, 2-port and ROM
  - High performance and area/power optimized version
  - Multiple periphery options

- POP™ IP
  - Cortex®-A57/A53
  - Mali™-T760

- GPIO
  - 3.3V and 1.8V versions
  - High density, fully programmable

Market & Solutions

- High-end Mobile
  - Optimized performance with stringent power/area budgets for world-class smartphones
  - State of the art power management features

- Server and Networking
  - High performance IP for compute and networking applications
  - Advanced feature set enables optimized system integration

- Implementation Solutions
  - POP IP for best in class performance and TTM
  - Family of Architect products for fast and reliable chip design

Availability

- Aggressive Schedule
  - Production quality EAC release available now

- Extensive Si Validation
  - Multiple functional testchips with Cortex-A57 and A53 successfully taped out and verified

ARM
ARM Artisan Optimized Implementation Solutions
Easing transition to 16nm FinFET process technology

**ARM Artisan Power Grid Architect**
- 60% Utilization

**ARM Artisan Signoff Architect**
- 80% +10% Utilization
- Area Reduction

Improving entitlement for area scalability

![Diagram showing delay variation vs. load/slew](image)

- Single slew/load point for SB-OCV
- Signoff Architect Coverage

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Complexity of 64-bit CPU implementation
- 64-bit CPUs need more engineering & compute resources
- ARM Cortex-A57 run-time in several days

16FinFET is exponentially more challenging to implement
- 16FF has ~2X more design rules than 28nm

“Winner takes all” – time-to-market is very important

Flexible solution
Address a wide variety of market segments

Reduce Risk
Leverage ARM expertise

Reduce Development Cost
Phy. IP + Scripts + Implementation Knowledge

Premium SoC Problems
ARM POP IP Enables New Era of Partnership

ARM POP IP

- SoC Designer
- Implementation Support
- RTL Optimization
- Process Optimization
- Foundry
- EDA Scripts
- EDA Flow

ARM Cortex-A CPU
Predictable Results in a Predictable Time-Line