Enterprise Trends

- IT is the business
- Density, power and cost over raw perf.
- One size no longer fits all
- Optimized highly integrated SoCs
- Open source and end user S/W
- Estimated 20x increase in network traffic
Networking Platforms and Compute Challenges

- Networking Infrastructure requires solving diverse problems in diverse platforms…
- Diverse platforms for diverse environments
  - Data center to shopping center!
  - Power efficiency and elasticity are always important
- Diverse compute problems
  - Demanding performance/efficiency requirements
  - Different cores for different problems
ARM’s Enterprise/Infrastructure “Triple Focus”

- Optimal performance and power efficiency with code portability across multiple silicon platforms
- Enabling new levels of efficiency through unlimited degrees of freedom for converged platforms
- Ability to “hit the right mix”
  - Compute, storage and networking in the right amounts
  - Standards based, open frameworks will enable innovation to thrive…

- Lead in Performance/Watt/Area
- Sustainable long-term processor architecture and ecosystem
Operators Require Revolutionary Infrastructure

- Better user experience
- Traffic driven demand for higher performance networking equipment
- Ubiquitous access and compute and cloud business models
- Flexible, yet standardized processing architecture
- Intelligence and management autonomy moving closer to users

Operator Pressures:
- Billions of M2M/IoT Connections; 8M Small Cells
- 17% of traffic is low-latency to cloud
- 100% Increase in Control signaling traffic
- 86% Operator power budget consumed by network
- New Business Models
- Network Growth
- CapEX and OpEX Efficiency
- Scalable and Optimized Deployments
- XaaS

Software Defined Infrastructure (SDN/NFV)
## Compute Domains in Networking

Interconnect must support all four

<table>
<thead>
<tr>
<th>Packet Processing</th>
<th>MAC Scheduling</th>
</tr>
</thead>
<tbody>
<tr>
<td>▪ Throughput driven (max throughput/W)</td>
<td>▪ Latency driven (real time control)</td>
</tr>
<tr>
<td>▪ Many cores</td>
<td>▪ Multiple cores</td>
</tr>
<tr>
<td>▪ I/O intensive</td>
<td>▪ Compute intensive</td>
</tr>
<tr>
<td>▪ Trend: Higher packet rates, more complex processing</td>
<td>▪ Trend: More complexity (LTE-A)</td>
</tr>
<tr>
<td>Small cores at maximum efficiency point</td>
<td>High single threaded performance cores</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Control Plane</th>
<th>Specialised Processing (L1, Content Delivery)</th>
</tr>
</thead>
<tbody>
<tr>
<td>▪ High single threaded performance</td>
<td>▪ Diverse requirements</td>
</tr>
<tr>
<td>▪ Legacy software, huge codebase</td>
<td>▪ Trend: More complex modulation schemes</td>
</tr>
<tr>
<td>▪ Trend: More complex signalling, machine to machine</td>
<td>DSPs, Accelerators</td>
</tr>
<tr>
<td>High single threaded performance cores</td>
<td></td>
</tr>
</tbody>
</table>

General-purpose cores may need to balance requirements across packet processing, control plane, scheduling
Scalable Platform for Diverse Processing Needs
Deployed in Cost-Efficient Power-Optimized Equipment
Ramping in Mid-range Performance for Enterprise

Set Top Box
Cable Modem
Home Gateway
DSLAM
Optical Line Termination
Cellular Small Cell Base Stations
Microwave Backhaul
SDN

Media content web
Mobile Broadband Access and Aggregation
Edge Router
Scale out storage
Core Router

ARM CORTEX
Processor Technology
Cortex-A57
Cortex-A53

ARM CORELINK
Processor System IP
CCN-504
Paradigm Shift for High Performance Networking and Server

ARM Cortex
Processor Technology

- Cortex-A57
- Cortex-A53

ARM CoreLink
Processor System IP

- CCN-508
- CCN-512

Cloud

- CDN
- RAN
- SGSN
- GGSN
- Edge Server

Network Equipment

- SDN
- Optical Core
- Cellular Macro Cell
- Base Stations

Email Web

- Evolved Packet Core
- HPC Core
- Storage Array Network Controller

HPC

- Scientific Compute
- Base Station Controller
- NFV

Set Top Box

- Gateway
- Storage
- Small Cell Base Stations
- SDN
Efficient Hardware Assisted Virtualization

- Direct hardware access with MMU-500
- Low latency interrupt delivery with GIC-500
- Support for on-chip or off-chip peripherals
Addressing Infrastructure Product Development

**ARM® DS**
Development Tools

- Single debug environment for full product life cycle

**ARM® CORESIGHT™**
Processor Debug & Trace IP

- Scalable and adaptable debug IP

- Cache visibility
- Multi-cluster SoC trace

- Trace-based flight recorder
- Software analysis

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### Efficient Interconnect for Compelling Scalable Solutions

<table>
<thead>
<tr>
<th>Approximate core count</th>
<th>Cost-efficient</th>
<th>Mid-range</th>
<th>High-end</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0MB</td>
<td>Level-3 Cache Size</td>
<td>32MB</td>
</tr>
<tr>
<td></td>
<td>20 GB/s</td>
<td>DDR Bandwidth</td>
<td>75 GB/s</td>
</tr>
<tr>
<td></td>
<td>2 Coherent ports</td>
<td>Coherent ports</td>
<td>24</td>
</tr>
<tr>
<td></td>
<td>0.2 Tb/s</td>
<td>On-chip bandwidth</td>
<td>1.8 Tb/s</td>
</tr>
</tbody>
</table>

- **Level-3 Cache Size**: 0MB, 32MB
- **DDR Bandwidth**: 20 GB/s, 75 GB/s
- **Coherent ports**: 2, 24
- **On-chip bandwidth**: 0.2 Tb/s, 1.8 Tb/s

**Efficient Interconnect for Compelling Scalable Solutions**

- **CCI-Kipling**
- **CCI-400**
- **CCN-502**
- **CCN-504**
- **CCN-508**
- **CCN-512**

**AMBA® 5 CHI**: CCN-504, CCN-508, CCN-512

**AMBA 4 ACE**: CCI-Kipling, CCI-400
ARM’s CCN Mixed Traffic Infrastructure SoC Framework

- Up to 4 cores per cluster
- Up to 12 coherent clusters
- Integrated L3 cache
- Quad channel DDR3/4 x72
- Virtualized Interrupts

Heterogeneous processors – CPU, GPU, DSP and accelerators

- Integrated L3 cache
- 1-32MB L3 cache
- Snoop Filter

Uniform System memory

- Up to 18 AMBA interfaces for I/O coherent accelerators and I/O

Peripheral address space

- Scalable architecture – 32/64 bit Heterogeneous Cores, Coherent Interconnect, Peripheral IP, Accelerator ports
- Virtualized capability
- Scalable Cache configuration and memory interfaces
Enterprise Networking Opportunity

e.g. Load balancers, Firewalls, SSL VPNs, Security and Intrusion Detection/Prevention

Layers 4 to 7

Layers 2 to 3

Wide range of rack-mount form factors

e.g. Switches and Routers

Server Class Application Processors

Network Processors

High Performance Packet Processing Processors

Fully Software Defined & Virtualized Functionality

ARM powered SoC

• n x Cortex-A57
• Next generation

• n x Cortex-A57
• n x Cortex-A53

• n x Cortex-A53
• Next generation
• Cortex-R/M

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Use Case Examples and Requirements

- Two examples that show NFV opportunities inside and outside the data center
- Visions for deployment of intelligence in the network
- Edge content delivery
  - Decentralization of core (server) functionality
- C-RAN/HetNet
  - Centralization of Radio Access Network functionality
  - Co-existence with current Macro and Small Cell base stations
Content Delivery at Edge

Benefits:

- Maximize bandwidth from existing fiber/backhaul by caching content close to the user
  - Cache in edge infrastructure (base station, G.Fast distribution point)
  - Cache in user equipment (home/enterprise router)
- Take advantage of application-specific knowledge, optimize across the stack
- Lower latency

Requirements:

- Standard OS + Virtualization environment for deployment of edge ‘apps’
- Server platforms in power-constrained environments
Macro Base Station (BTS) SoC

16 cores – Data/Control plane

- A57
- A57
- A57
- A57

CCN-504, CCN-508

Offload

- A53
- A53

8 cores – Data plane offload

- DSP
- DSP

- DMC

Server-class compute 64-bit, Virtualisation

- Crypto
- Work Scheduler
- Buffer Manager
- Timer Manager

Accelerators with Open Data Plane interface

PCIe

Network Ingress

Network Egress

DMC

16 cores – Data/Control plane

8 cores – Data plane offload
C-RAN/HetNet

Benefits:

- **Optimize Radio Access Network**
  - Backhaul availability (Fiber or uWave)

- **Efficiency from consolidation**
  - For example, where peak loads are offset in time (residential/business)

- **Efficiency from heterogeneity**
  - For example consolidate all packet processing onto specialized silicon

Requirements:

- **OEM ability to maintain same software stack for multiple silicon platforms**

- **Scalable platforms (few-many cores) for low power consumption at the edge, and high efficiency in the data center**
Future C-RAN/Server

- DMC
- Network Ingress
- Network Egress
- DSP
- Timer Manager
- Buffer Manager
- Work Scheduler
- Consolidated Compute Server, MAC Scheduling

Software packet processing (small cores)

CCN-512 and future

Accelerators with Open Data Plane interface
Value of ARM ecosystem in networking is the differentiated IP developed by ARM’s partners
  - Traffic manager
  - Work scheduler
  - Baseband, cryptography

Differentiation necessary to support the diverse requirements
Standardization necessary to enable Open Source Software and NFV use-cases
Standard OS + Virtualization environment for deployment of edge ‘apps’ → SBSA
OEM ability to maintain same software stack for multiple silicon platforms → Open Data Plane
Data Plane

- Data plane APIs fragmented across the entire industry
- Need for standardization to meet next-generation requirements
- Need an open standard for flexibility, choice and adaptability
- Standardization must allow innovation and differentiation for different parts of the network
  - OpenGL a good example from a different domain
- Standardize access to hardware accelerators that have:
  - Common functionality, but different implementations
  - Significant benefit(s) in performance, scalability or isolation
- Setting the right level of abstraction requires collaboration
  - ODP being developed in a public forum (Linaro LNG) with direction from ARM, OEMs and silicon partners
OEMs, ISVs get true portability for apps & middleware!

Standardized data plane API to enable Linux-based networking applications across any architecture

- Open support for ARM, x86, MIPS & PowerPC!

Structured to enable future innovation

- Lightweight abstraction preserves performance w/o compromise
- Access and management of HW accelerators
- Supports optional schedulers to provision easy management and traffic load balancing

Proprietary SDKs sit underneath for OEM/ISV software platform simplification (e.g. Supports DPDK on x86)
Standardization in Networking: An Example

The SBSA standardizes interface to non-differentiating hardware

Operating system vendors target a single system image to all SBSA compliant hardware

Open Data Plane standardizes API for different implementations of common networking accelerators
- Queues
- Buffers
- Crypto accelerators
- Classification accelerators

Application vendors target a single API
Core and Interconnect Challenges

- Compute problems and platform constraints necessitate different types of cores
- Server platforms in power constrained environments → ARM Cortex-A57, ARM Cortex-A53
- Scalable platforms (few-many cores) for low power consumption at the edge, and high efficiency in the data center → CCN-family
- Big distinction from ARM big.LITTLE™ in the mobile world!
  - Cores for different types of workloads, not the same workloads at different performance points
- Virtualization (and other A-profile features) needed everywhere…
- Interconnect needs to scale across many system sizes, and support accelerators, I/O
ARMv8-A Infrastructure Ecosystem Building Momentum
ARM Networking Progress to 2014…

- Transition major players in the silicon ecosystem to ARM
  - Possibilities from full COTS, to merchant silicon, to FPGA

- ARM-based Cortex-A15 platforms shipping
  - Realization of flexibility and efficiency benefits for the base station market

- Linaro Networking Group
  - Influencers and end users working together to solve real-world problems

- ESTI NFV Working Group
  - ARM and partners working with Carriers to enable open, standardized frameworks for rapid innovation of networks

- Open Data Plane (ODP) and Server Base System Architecture (SBSA)
  - Open source initiatives launched to enable open, standardized software frameworks

- Expanding roadmap for ARM Cortex and CoreLink products

Significant (70%+) Base Station (Baseband and Radio head) market share
Summary: ARM Resolving the Needs of Infrastructure

- Enabling a silicon partner ecosystem with best in class compute and interconnect IP for highly integrated SoCs
- Enabling infrastructure expansion with lower total cost for compute; a choice of optimized hardware across broad performance, price, and power requirements of heterogeneous networks
- Enabling **portability** of **software** and **workloads** for the era of rapidly evolving services

- Linaro
- Virtualization
- Optimal Integration:
  - PoC Delivery platform
  - Linux
  - Open Source
  - Carrier Grade
- Silicon Choice
- Multi-core
- High-Performance Interconnect
- Heterogeneous Processing
- Performance/mW