Cadence Mixed-signal/Low-Power Flow for Embedded ARM® Cortex®-M0 Designs

2014 ARM 物理IP技术研讨会
Trends driving MS and LP design needs
Mixed-signal is pervasive throughout applications experiencing dramatic market growth

Mobility
- Wireless connectivity / broadband
- Compact size, handheld, thinner, lighter
- Battery operated
- Performance and features

IoT/Home /Industrial automation
- Smart sensors and metering
- Microcontrollers everywhere
- Everything connected (Internet of every thing)
- Health monitors and medical devices

Automotive
- Safety
- Reliability
- Fuel /electrical efficiency
- Infotainment and convenience
ARM® Cortex®-M0 Processor

- Easiest way to get started with Cortex-M processors
  - Smallest and most accessible Cortex-M processor family
  - Access wide ARM ecosystem
  - Get to silicon faster with the System Design Kit
  - Upwards compatible with all Cortex-M processor family

- Add a sophisticated processor into your design
  - Performance headroom for advanced features
  - Longer battery life through efficient 32-bit architecture
  - Reduced system cost through code density

- Extends ARM architecture to new applications
  - Mixed signal devices
  - IoT end points
Integrated MS Flow for Embedded Cortex-M0

- Debug system across HW / SW and analog / digital boundaries
- Optimize system partitioning
- Model analog functionality using simulation-efficient RNM
- Model power reduction strategies
- Verify power intent using static and dynamic methods
- Use advanced verification methodology
- Explore floorplan option for best area and power
- Implement AMS blocks in OA-integrated mixed-signal flow
- Manage ECOs effectively at any stage of design
Design Flow for embedded Cortex-M

System Specifications

- Testbench
- Analog Models
- Low Power Intent (CPF)
- AMS IP

Virtuoso Schematic and ADE
- Incisive/AMSD Simulation and Verification

Verified Design

Virtuoso-EDI OA integrated flow
- Floorplanning
- Analog Block
- Digital Block
- Chip Integration
- Signoff

Cortex-M System Design Kit (CMSDK)
- Cortex-M RTL (Verilog)
- ARM DS-5 and ARM Keil® Software Development
- ARM Artisan® physical IP
- Flash Memory
- SRAM

Provided by Cadence
Provided by ARM
Provided by 3rd Party
Block Diagram of the Control System
Representative Mixed-Signal Device

Design Domains

Block Diagram
Analog Interface to Cortex-M System Design Kit

CM SDK Example

Peripheral (APB) Subsystem

- UARTs
- Timers
- Watchdog

Analog Interface
- DAC
- ADC

Addition to CM SDK

16-bit data + ctrl

AHB™ to APB Bridge

AHB™

Cortex-M0

ROM
RAM
GPIO
Default Slave
Embedded Cortex-M0 Flow Modules

- Describe Automotive Sensor System in VSE
- Model analog block (DAC) in RNM (wreal) using SMG
- Compile C code into processor instruction set using Keil
- Run functional RNM/SPICE/RTL/SW Simulation from Virtuoso ADE in Incisive for different scenarios and present results in SimVision
- Run CPF-driven AMS simulation by Incisive
- Export CPF for Custom part and top level using VSE PIEA
- Run structural Low Power checks from VSE using CLP
- Create top level chip floorplan in VFP
- Analog block (DAC)
  - schematic design
  - RNM vs schematic model validation
  - Physical layout
- Digital Block (Cortex-M0)
  - RTL and Test synthesis by RTL Compiler; equivalency checking by Conformal
  - P&R using VDI-XL in OA abstract passed from Virtuoso;
  - Bring implemented digital block back to Virtuoso using OA
- Chip Integration and Sign-off
Pressure/Temperature Control System
in Virtuoso Schematic Editor (VSE)

Pressure range: 0 to 120 psi
Nominal pressure: 78 psi
Normal operating range: 75-82 psi
Temperature range: -40 to 100 °C
Analog Behavioral Model Generation and Validation

- Building blocks are placed, wired, configured, and calibrated using Virtuoso Schematic Editor
- No need to write code
- Model-schematic can be reused, shared, reconfigured, and maintained
- Easily understandable graphical representation of the design functionality
- Less dependent of language and modelling skills of an engineer
- Model Validation Flow integrated in Virtuoso ADE-XL (amsDMV)
Results of System Simulation

Temperature = 0°C
Initial Pressure = 0 psi
System clock = 50 MHz (clk)
ADC Sampling Event = 128 clk (2.56us)
System achieves 78 psi in 28 cycles
Simulation and Debugging w/Software Trace

- Analog Waveform
- Digital Waveform
- C Code
- Assembly Code
CPF Controlled Mixed-Signal Simulation

directly provide power supply to analog power domain
CPF Controlled Mixed-Signal Simulation
CPF Generation from Schematic

Virtuoso Power Intent Export Assistant (PIEA)
Schematic-Driven Physical Implementation Flow

- Top Level Floorplan
- Analog/Custom Blocks
- Top Level
- Chip Integration & Signoff

OpenAccess

RTL netlist
Library
Constraints

Synthesis
Test Insertion
Floor planning
Power Planning
Clock Tree
Routing
STA
Physi. Verification

Invoke customizable script for digital block implementation from Virtuoso
Chip Floor Planning in Virtuoso

Schematic-driven layout: You start from here.

Input

- Configure Physical Hierarchy to use preliminary floorplan views
- Generate Physical Hierarchy (top and soft blocks)
- Block Placement, Pin Optimization, Pin Alignment
- Level-1 Editing for block PR boundary and pins

Output

Dynamic measurement to adjust PR boundary:

```
dx : -37.0050
dy : 0.0000
deg : 12286.9462
Utilization : 1.4799
```
Initial Floorplan in Virtuoso-XL
RTL Synthesis and DFT Insertion Flow

- Low Power Synthesis of Cortex-M0 System (CPF driven)
  - Includes Cortex-M0 Integration level core
  - AMBA® AHB Lite interface to external ROM and RAM
  - Power management unit
  - Clock Control & IO

- Test Insertion in RC cockpit
  - Insert Full Scan and Compressed Scan (2 SI/2SO)
  - Isolate Digital Core (from Analog) with IEEE1500
  - Insert Test Points to improve Coverage (RRFA analysis)
  - Insert Wrapper logic for embedded ROM and RAM
  - Implement Direct Access LBIST for Post-manufacturing

- Validation & Pattern Generation
  - Verify synthesis Netlist using Conformal Low Power/LEC
  - Verify Test Structures
  - Generate ATPG patterns and Signature for LBIST
  - Validate patterns in Incisive
Partnership for Success

ARM
- Compact, energy efficient processors
- Optimized physical IP
- System IP

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Cadence
- Integrated flow for mixed-signal design
- Low power design and verification
- Analog and mixed-signal IP

Mixed-Signal Device
- Productivity
- Quality of silicon
- Time to market
- Smart Analogue
- IoT

Mixed-signal Device