Physical IP Solutions for Internet-of-Things and Mobile Applications

ARM Physical Design Group
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Market Trend: Analog Devices Become Smart

- Digital control and signal processing lead to “Smart Analog” with much higher functionality and power efficiency.
  - Smart sensors, motor control and power management

- End points for Internet of Things (IoT) are typically connected analog
  - Sensors integrated with a controller for signal processing and communication.

- Area & power efficient physical libraries are critical
  - Enable low cost Embedded & IoT SoC implementation for extended battery life
IoT & Embedded SoC Design Challenges

- Radio, MCU, Sensor
  - Integrated analogue + power management + display drivers + sensors
  - Integrated wired & wireless connectivity

- Integrated NVM (emFlash)

- Energy efficiency

- Low cost

- SoC Mixed-Signal Design implementation methodology
ARM Cortex Processor family

Cortex-M0
- “8/16-bit” applications
- Lowest cost

Cortex-M0+
- “8/16-bit” applications
- Lowest power
- Outstanding Energy efficiency

Cortex-M3
- “16/32-bit” applications
- Performance efficiency
- Feature rich connectivity

Cortex-M4
- “32-bit/DSC” applications
- MCU plus DSP
- Accelerated SIMD, FP & SP

Consistent architecture across all applications

Cortex-M
- Energy Efficient
- Ease of Use
- Configurable
- Deterministic
- Low Silicon Area
- WIDELY ADOPTED
- MARKET PROVEN
- HIGH VOLUME
# ARM Cortex-M0+ Benchmarks x Node

<table>
<thead>
<tr>
<th>PPA</th>
<th><strong>180ULL</strong> (7-track, typical 1.8v, 25C)</th>
<th><strong>90LP</strong> (7-track, typical 1.2v, 25C)</th>
<th><strong>40G</strong> (9-track, typical 0.9v, 25C)</th>
<th><strong>28HPM</strong> (9-track C35 HVt, typical 0.9v, 25C)</th>
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<td>Area</td>
<td>Power (Dhrystone loop)</td>
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<td>Minimum Config*</td>
<td>0.13mm²</td>
<td>52µW/MHz</td>
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<td>Feature Rich Config**</td>
<td>0.27mm²</td>
<td>76µW/MHz</td>
<td>0.08mm²</td>
<td>17µW/MHz</td>
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<th>Max Freq</th>
<th><strong>40G</strong> (12-track RVt, typical 0.9v, 25C)</th>
<th><strong>28HPM</strong> (12-track C31LVt, typical 0.9v, 25C)</th>
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<tr>
<td>Feature Rich Config**</td>
<td>753MHz</td>
<td>896MHz</td>
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</table>

For all trials: 50Mhz target frequency

* Minimum Config: 1 IRQ, small multiplier, no WIC, 0 bkpt, 0 watchpt
** Feature rich Config: 32 IRQ, fast multiplier, WIC, Systick, 4 bkpts, 2 watchpt

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<tr>
<th>DMIPS/MHz</th>
<th>CoreMark/MHz</th>
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<td>1.31*</td>
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Typical Cortex-M0+ implementation w/nominal Vt
Artisan Physical IP Around the SoC

**POP™ IP**
- Core-hardening acceleration technology
- Implement power or performance optimized Cortex® solutions

**Standard Cells**
- Multiple track height libraries
- Multi-Vt cell libraries
- Multi-Channel cell libraries
- TGO libraries

**Memory Compiler**
- Next generation Artisan® memories
- High speed & high density
- Multiple low power/retention modes

**Interface**
- GPIO
- Architected for low power
- High density multi-row capabilities

**POP IP**
- Core-hardening acceleration technology
- Implement power or performance optimized Mali™ GPU solutions
State-of-the-Art Support of EDA Flows

- Synthesis
- Floorplanning
- Placement
- CTS
- Test Insertion
- Routing
- ATPG

- Simulation
- LEC
- DRC/LVS/DFM
- Timing Analysis
- Signal Integrity
- Power/IR Analysis

Apache
ARM Offers the Broadest Foundry Solution

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<tr>
<th>Company</th>
<th>16/14nm FinFET</th>
<th>20nm</th>
<th>32nm 28nm</th>
<th>45nm 40nm</th>
<th>55nm</th>
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[DesignStart™ Online Access to ARM IP](designstart.arm.com)
# IoT & Embedded SoC Process Nodes for MCU/CPU

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- **32/64-bit Applications Processors**
- **Embedded / IoT**
- **Real-time + DSP Cores**
- **3/16/32-bit Cores**
IoT & Embedded SOC Implementation x Process Node

- **BCD/HV**
- **Analog M/S**
- **uLL TGO Logic**
- **Ultra-low Power Memory**
- **Embedded MCU/Flash**
- **Base CMOS Logic**

**More than Moore**

- **Motor Control**
- **Battery Monitoring**
- **LED Lighting**
- **PMIC**
- **Sensor Networks**
- **Touch-screen Controllers**
- **Stability Control**
- **Body control Sensors**
- **Tire pressure Sensors**
- **Body Control Pressure Intruder Sensors**
- **Medical Electronics**
- **Smart Meter**
- **eDashboard**
- **<256K Embedded Flash**
- **>4M Embedded Flash**
- **Real-time MCU**
- **Apps Processor Core**
- **Embedded MCU**
- **90-180nm**
- **55/65nm**
- **40→28nm**

**Moore’s Law**

- **Infotainment**
- **ABS/Airbags**
- **Electronics Stability Control**
- **Wearable Devices**
- **IoT Connected Devices**
- **Battery Monitoring**
- **Tire pressure Sensors**
- **Pressure Intruder Sensors**
- **Body control Sensors**
- **Sensor Networks**
- **Real-time MCU**
- **Motor Control**
- **Battery Monitoring**
- **LED Lighting**
Optimized IoT Platforms

- New Thick-Gate Oxide (TGO) platforms
  - Covering 90nm to 180nm
  - Suited for very low power designs

- New IoT-optimized physical IP for 55nm process technologies
  - Optimal balance between low power, cost and performance
  - ARM IP for multiple foundries
Physical Design Solutions for Always On and Low Power

- Ultra-high density multi-channel libraries for low cost and power
- Optimized Power Management
- Deep N-well for noise immunity
- Area optimized memories
- Reduced leakage standby modes
- Very low voltage assist circuits
- Thick-Gate Oxide (TGO) Library for low-leakage always-on blocks
- Optimal integration with analog sensors and controllers
- Direct interface to Li-ION batteries

Diagram of a chip with the following components:
- Memory
- Always-on Block
- Cortex-M Processor
- Analog IP
- Regulator
- Embedded Flash
- I/O Cells
Benefits of TGO Logic
Extended Operating Voltage Range & Reduced Leakage Power

TGO device provides significantly lower leakage than standard device
Power Management Kit (PMK)

- Contains power gates, level shifters, retention flops etc

- PMK enables both active and leakage power mitigation

- Fits into standard EDA flow with support for both UPF and CPF

➢ Save up to 80% in processor leakage using PMK
Retention Flops to Save State

1. D-flop main stage (SVт or LVт)
   - Connects to switchable (local) power rails

2. D-flop retention stage (HVт)
   - Connects to global (always-on) power
Next Generation Memories Optimized for IOT based SOC Design

- **Highest densities AND low power**
  - Up to 33% denser than competition—HD Compilers

- **HD Compilers - 400MHz**;
  - Optimal for relevant market segments like IoT, embedded, MCU, Bluetooth etc

- **Features minimizing impact on baseline PPA**
  - New features like embedded scan chains to reduce ATPG effort/enhance fault coverage and wake–on–access to reduce leakage
  - Simplification of unused features like pipeline, etc.
Range Extension of SP-RF & SP-SRAM

For memory size 32kb-256kb, range extension provides significant area + power savings

- Range extension of Register File provides significant area & power reduction for Embedded & IOT program execution

*All comparisons v/s Single Port SRAM
Memory Power Management Modes

- Source biasing (integrated footer in memory) to reduce retention leakage (up to additional 30%)
- RF applications ready – supports thick metal 5
- HVt implant in HD memory compiler periphery to minimize standby leakage
- Multiple sleep/nap modes for multiple leakage retention modes – standby, wake on access, retention and power down

➢ Multiple state retention modes enable power-optimized IOT based SOC design
Leakage vs. Wake Up Time

- Up to 55% leakage reduction using retention modes
## Power Optimized Designs Enabled

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<tr>
<th>Feature</th>
<th>Dynamic Power Control</th>
<th>Leakage Power Control</th>
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<td>Clock gating standard cells</td>
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<tr>
<td>• No dynamic power on FF’s</td>
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<td>Extended operating range</td>
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<td>• Lower voltages for timing uncritical blocks</td>
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<td>• Voltage level shifters as interface</td>
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<td>• Digital voltage and frequency scaling (DVFS) support</td>
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<td>TGO libraries</td>
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<td>• Leakage reduction for “always-on” blocks</td>
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<td>• Wide operating range for direct interface to battery &amp; sensors</td>
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<td>Multi Vt support in standard cells and memories</td>
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<td>• High Vt (low leakage) cells with reduced performance in uncritical paths</td>
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<td>Power gating and power down modes in memories</td>
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<td>• Flexible power saving modes</td>
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<td>Power gates for logic blocks</td>
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<td>• Shut-down of parts of the design</td>
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<td>• Minimal leakage current by maintaining FF state w/o loss of performance in normal mode</td>
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<td>Back-bias support</td>
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<td>• Minimal leakage current for inactive or low performance blocks</td>
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**Flexible combination of Power Management functions depending on design goals**
Advanced Memory Test & Repair Features

**ARM Artisan Next-Generation Memories**

- **Comprehensive Testing & Diagnosis**
  - Deep submicron process nodes from leading and emerging foundries require advanced test & yield diagnostics performed at speed
  - Physical & logical mapping and ATPG combined with standard & user-defined test algorithms drives repair effectiveness

- **Repair Analysis and Self-Repair**
  - Repair process partially or fully on-chip
  - Allows area, test time & yield trade-off

- **Advanced Design Automation**
  - Key to supporting SoCs with large number of memory subsystems and 100s memory of instances
  - Fully automated & integrated BIST/R insertion

- **ARM Core BIST interface support**

- **Mentor and ARM ensuring full interoperability between Tessent MemoryBIST and ARM physical memory IP**
  - Memory views and Artisan memories available from ARM
  - Tessent tools available directly from Mentor

![Diagram of ARM Artisan Next-Generation Memories](image)
ARM Artisan Test Chip Overview

- Goals
  - Verify AC/DC/parametric functionality
  - Correlate models and simulation results
  - Exercise EDA views and tools
  - TSMC Compliance and Test Chip Report

- Memory - Test Overview
  - Many instances per compiler
  - Tall, wide, big, small, typical
  - BIST ‘at speed’ testing on one instance/compiler
  - Access time, set-up, and hold time one instance/ compiler
  - Power measurement

- Memory - Functional Test and Yield
  - PVT splits (SS, SF, TT, FS, FF)
  - Set-up and Memory access time
  - Compare against appropriate .lib corner
  - Power Measurements
Starting Point for Physical IP Evaluation

- >130 unique Physical IP Platforms
  - Free IP evaluation
  - Most Memory & Logic IP available at no cost

http://designstart.arm.com
Partnering to provide industry leading IOT & Embedded SoC design solutions

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Thank You

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