## Certificate





No.: 968/FSP 1923.00/20

Product tested General purpose microprocessor

design including safety features

Certificate holder

ARM Ltd.

110 Fulbourn Road Cherry Hinton Cambridge CB1 9NJ United Kingdom

Type designation ARM Cortex-R52 Processor IP Core

Revision r1p1 and r1p2

Codes and standards IEC 61508 Parts 1-7:2010 (in extracts) ISO 26

ISO 26262 Parts 1-10:2011 (in extracts)

Intended application The ARM Cortex-R52 Processor IP Core complies with the requirements of

IEC 61508 for SIL 3 regarding the avoidance of systematic faults for a Compliant Item and complies with the requirements of ISO 26262 for ASIL D regarding the avoidance of systematic faults for a Safety Element out of Context (SEooC). Based on an exemplary configuration, ARM showed that the target values for the random hardware fault metrics according to ISO 26262-5, Clauses 8 and 9 for ASIL D can be met. As a result this Cortex-R52 Processor can be used in safety-related applications up to SIL 3 according IEC 61508 and up to ASIL D according to

ISO 26262.

Specific requirements The requirements and constraints mentioned in the Cortex-R52 Safety Manual have

to be taken into account by the user.

Valid until 2025-10-26

The issue of this certificate is based upon an examination, whose results are documented in Report No. 968/FSP 1923.00/20 dated 2020-10-21.

This certificate is valid only for products which are identical with the product tested.

TÜV Rheinland Industrie Service GmbH

Bereich Automation
Funktionale Sicherheit

Köln, 2020-10-26

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Certification Body Safety & Security for Automation & Grid

Dr.-Ing. Thorsten Gantevoort



