

Errors in “The Definitive Guide to the ARM Cortex-M3”

28-July-2008

Page xviii, second item in bulletin list:

“Assembly code in generalized syntax; items inside < > must be replaced by real register names:”

Page 36 (near bottom of the page)

“The CONTRL[0] bit...” should be “CONTROL[0] bit...”

Page 41 (near top of the page)

“The address 0x00000000 is used as the starting value for the MSP.”

This should be

“The address 0x00000000 is used to store the starting value for the MSP.”

Page 42

Due to an editing error, the diagrams on this page are incorrect. The following are the corrected diagrams:

Main Program

```

...
; R0 = X, R1 = Y, R2 = Z
BL   function1

; Back to main program
; R0 = X, R1 = Y, R2 = Z
... ; next instructions

```

Subroutine

```

function1
    PUSH    {R0-R2} ; Store R0, R1, R2 to stack
    ... ; Executing task (R0, R1 and R2
        ; could be changed)
    POP     {R0-R2} ; restore R0, R1, R2
    BX     LR ; Return

```

Figure 3.11 : Stack Operation basics: Multiple Register Stack Operation

Main Program

```

...
; R0 = X, R1 = Y, R2 = Z
BL   function1

; Back to main program
; R0 = X, R1 = Y, R2 = Z
... ; next instructions

```

Subroutine

```

function1
    PUSH    {R0-R2, LR} ; Save registers
                        ; including link register
    ... ; Executing task (R0, R1 and R2
        ; could be changed)
    POP     {R0-R2, PC} ; Restore registers and
                        ; return

```

Figure 3.12 : Stack Operation basics: Combining Stack POP and RETURN

Page 68, table 4.26, the “or” should be “and”

Symbol	Condition	Flag
GE	Signed greater	N set <u>and</u> V set, or N clear and

	than or equal	V clear (N == V)
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Page 92 : Bit-band vs Bit Bang box

“Bit-band commonly refers to driving I/O pins under software control to provide serial communication functions.” should be

“Bit-bang commonly refers to driving I/O pins under software control to provide serial communication functions. “

Page 116, table 7.1, improvement and correction in descriptions

Exception number	Exception type	Priority	Descriptions
11	SVCall	Programmable	System Service Call <u>(or Supervisor Call)</u>
14	PendSV	Programmable	Pendable request for system <u>services</u>

Page 150, “N-32 (0 X 20)” should be “N-32 (0x20)”

Page 188, the “N” in the following text should be in superscript

“ $R_n + 2N * R_m$ ” should be “ $R_n + 2^N * R_m$ ”

Page 245, step 4 of reading a core register should be

“4. Read the DCRDR to get the register content.”

Page 257, table 16.2

Title of the table should be “Cortex-M3 Default ROM Table Values”

Page 332, table C-2

“(Nv12)” should be “(N-12)”

Page 342

Unexpected thin line on top of table D.30

Back cover

“Cortex M-3” should be “Cortex-M3”

[End of Document]