

ARM® CoreSight™

ARM CoreSight™ technology provides a complete debug and trace solution for your entire system-on-chip (SoC). It makes single ARM core and complex multi-core SoCs easy to debug and thus speeds development of high quality ARM Powered® products.

CoreSight technology builds on ARM's current Embedded Trace Macrocell™ (ETM™) products, which are widely licensed and supported by ARM RealView® development tools and all other leading tool vendors.

Key Benefits

- Higher visibility of complete system operation through fewer pins
- Standard solution across all silicon vendors for widest tools support
- Re-usable for single ARM core, multi-core or core and DSP systems
- Enables faster time-to-market for more reliable and higher performance products
- Supports highest frequency processor and low energy SoC
- The industry name for on-chip debug and trace

Devices implementing CoreSight technology can comply at four independent levels.

CoreSight Debug

Debug Access Port

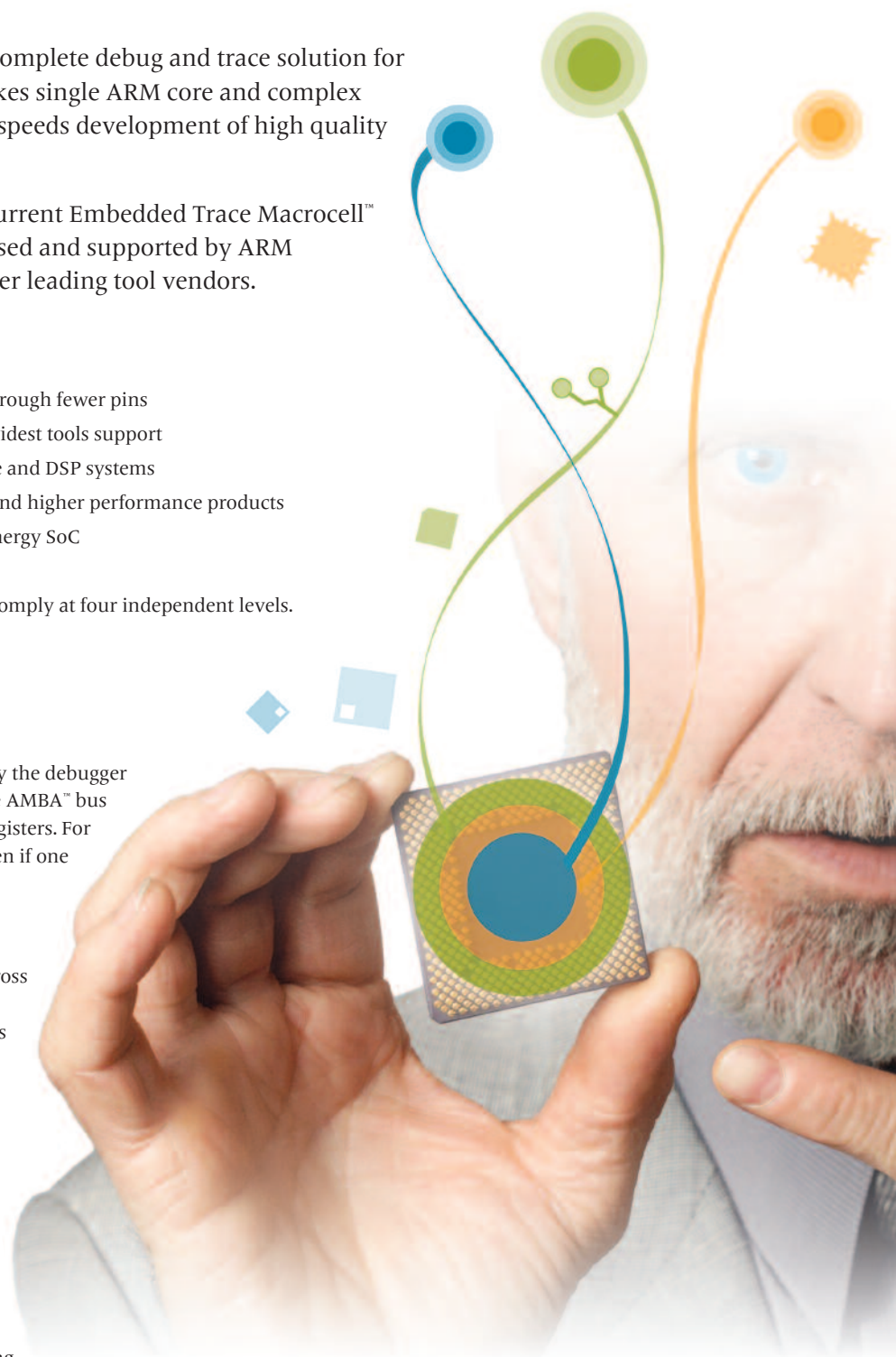
The Debug Access Port provides real-time access by the debugger software to the JTAG scan chains in the chip, to the AMBA™ bus system and to all debug and trace configuration registers. For multi-core systems debug access is maintained even if one core powered down or asleep.

Embedded Cross Trigger (ECT)

The ECT consists of a Cross Trigger Matrix and a Cross Trigger Interface block. The Cross Trigger Matrix provides system wide channels for debugging events to be passed between cores or ETMs. The Cross Trigger Interface provides the shaping and control logic to connect the debug events onto each channel in the matrix.

CoreSight ETM

The CoreSight ETM monitors the core's internal buses allowing information on the processor activity (program and data) to be captured both before and after a specific event, while adding no burden to the processor's performance and enabling the core to run at full speed. New higher data compression squeezes full program trace down to an average of only 1-bit per CPU cycle.



The ARM logo, consisting of the letters 'ARM' in a bold, blue, sans-serif font, with a registered trademark symbol (®) to the upper right.

Powerful software-configurable filters and trigger logic allow the developer to precisely select which instructions and data are captured by the ETM before the information is compressed. The compressed data is either passed directly off-chip through a dedicated, configurable, Trace Port Interface Unit or can be stored in the Embedded Trace Buffer™ (ETB™) for later read-out.

The CoreSight ETMs are supplied with ETM JTAG Port and ETM Trace Port blocks for backward compatibility as drop-in replacement for existing single ETMs.

CoreSight ETMs are available for the ARM9E, ARM11 and Cortex core families. These conform to the new ETM v3 architecture and support cores with TrustZone™, Thumb™-2 and Intelligent Energy Manager (IEM) technologies.

CoreSight Multi-source Trace

Trace Funnel

The CoreSight Trace Funnel is used to combine multiple trace sources into a single bus, called the AMBA Trace Bus (ATB). An arbitration and prioritization scheme is used to select the input trace stream to pass for each bus cycle.

Embedded Trace Buffer

The CoreSight Embedded Trace Buffer (ETB) is used for storing trace data on-chip at high rates and at 32-bit data width. The data can then be read-out at a lower rate — either through the Debug Access Port or by the ARM processor. The ETB enables trace information to be analyzed where the number of pins and/or frequency of the required trace port is unacceptable.

The CoreSight ETB provides a memory interface suitable for compiled 4K-1Mbytes of SRAM (supplied by the semiconductor manufacturer).

Trace Port Interface Unit

The CoreSight Trace Port Interface Unit formats and transmits trace data off-chip at frequencies asynchronous to the core. The trace data format embeds a source ID into a byte stream to enable multiple trace sources to be transmitted through a single trace port. The trace port is configurable at synthesis and by software to vary the width from 2 to 34 pins and the frequency from 1KHz to the maximum supported by the target process and I/O cell library.

AHB Trace Macrocell

The AMBA AHB Trace Macrocell gives visibility to bus information, not inferable for core trace using an ETM, including:

- System performance statistics.
- Multi-layer bus utilization.
- Visibility of access to memory areas.
- Break or trigger signals to the ECT

Instrumentation Trace

The CoreSight Instrumentation Trace provides an efficient mechanism for instrumented code running on the target to generate a high level trace. Software running on the ARM processor can write to a block of 32 word registers and this data will be output into the Trace Funnel

for combining with other trace data or alternatively via the Single Wire Viewer (see below).

CoreSight Serial Wire

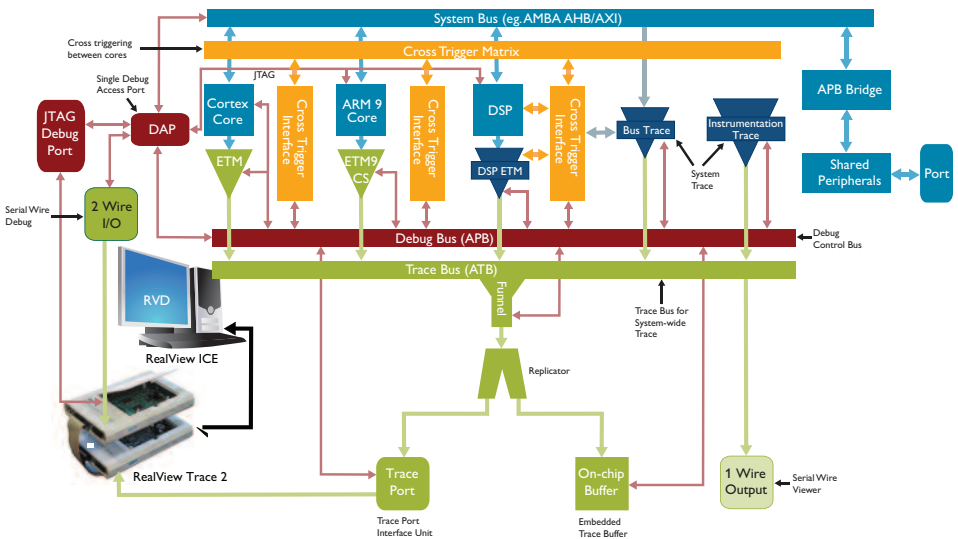
CoreSight Serial Wire Debug makes debug affordable in end-product with a mature multi-drop 2-pin debug solution, equivalent but highest performance than 5/6 pin JTAG interface.

The CoreSight Serial Wire Viewer provides an output for Instrumentation Trace through a single pin. The output is unidirectional using Manchester encoding to transmit clock and data over a single wire.

CoreSight Serial Wire Debug provides a 2-pin equivalent to 5/6 pin JTAG interface with connection via the Debug Access Port

CoreSight Design Kit

The CoreSight DK9, DK11, DK-R4, DK-A8, DK-A9 and now DK-A5 design kits include all of the above components. Deliverables include Verilog design simulation models, full documentation and system level Integration Kit for functional validation of the CoreSight components within the customer specific SoC design.



Do a Google search for this product

Search term: ARM CoreSight

Web:

www.arm.com/products/solutions/CoreSight.html

Call us

CHINA
+86 21 62351296

FRANCE
+33 1 39 30 47 89

GERMANY
+49 89 928 615 0

INDIA
+91 80 5138 4000

ISRAEL
+972 9 7632000

JAPAN
+81 45 477 5260

KOREA
+82 31 712 8234

NORWAY
+47 4000 5757

SINGAPORE
+65 6728 0950

TAIWAN
+886 2 2627 1681

UK
+44 1223 400400

USA
+1 408 576 1500

ARM, ARM Powered, StrongARM, Thumb, Multi-ICE, ModelGen, PrimeCell, PrimeXsys, RealView, TrustZone, Jazelle, ARM7TDMI, ARM9TDMI, ARMulator AMBA, and The Architecture for the Digital World are registered trademarks of ARM Limited. Cortex, AXI, AHB, ARM7, ARM7TDMI-S, ARM7EJ-S, ARM720T, ARM740T, ARM9, ARM9TDMI, ARM920T, ARM922T, ARM940T, ARM9E, ARM9E-S, ARM926EJ-S, ARM946E-S, ARM966E-S, ARM968E-S, ARM996HS, ARM10, ARM1020E, ARM1022E, ARM1026EJ-S, ARM11, ARM1136J-S, ARM1136JF-S, ARM1156T2-S, ARM1156T2F-S, ARM1176JZ-S, ARM1176JZF-S, EmbeddedICE, EmbeddedICE-RT, AMBA, ARM Development Suite, ETM, ETM7, ETM9, ETM10, ETM10RV, ETM11, Embedded Trace Macrocell, Embedded Trace Buffer, ETB, ETB11, Embedded Trace Kit, Integrator, JTEK, Mali, MultiTrace, MPCore, MOVE, OptimoDE, AudioDE, SecurCore, SC100, SC110, SC200, SC210 are trademarks of ARM Limited. Java is a trademark of Sun Microsystems, Inc. XScale is a trademark of Intel Corporation. All other brand names or product names are the property of their respective holders. "ARM" is used to represent ARM Holdings plc (LSE: ARM and NASDAQ: ARMHY); its operating company ARM Limited; and the regional subsidiaries: ARM, Inc.; ARM KK; ARM Korea Ltd.; ARM Taiwan Limited; ARM France SAS; ARM Consulting (Shanghai) Co. Ltd.; ARM Belgium N.V.; AXYS Design Automation Inc.; ARM Germany GmbH; ARM Embedded Technologies Pvt. Ltd.; ARM Norway, AS; and ARM Sweden AB. Neither the whole nor any part of the information contained in, or the product described in, this document may be adapted or reproduced in any material form except with the prior written permission of the copyright holder. The product described in this document is subject to continuous developments and improvements. All particulars of the product and its use contained in this document are given by ARM in good faith. All warranties implied or expressed, including but not limited to implied warranties of satisfactory quality or fitness for purpose are excluded. This document is intended only to provide information to the reader about the product. To the extent permitted by local laws ARM shall not be liable for any loss or damage arising from the use of any information in this document or any error or omission in such information.