Cortex-A76AE

Automotive Enhanced

arm

Datasheet

Benefits

1. **Thermal Efficiency**

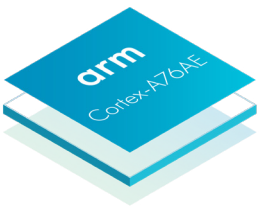
   Contains the latest state-of-the-art microarchitecture features that deliver greater single-thread integer, floating-point, memory and ML performance. Executes workloads with sustained performance within constrained power envelopes.

2. **Flexibility with Split-Lock**

   Switch between split mode for highest multicore performance or lock mode for advanced multicore fault-tolerance with ASIL D hardware metrics. Provide additional flexibility for future mixed-criticality applications.

3. **Superscalar Processor Core**

   The superscalar processor core decodes, issues, and executes more instructions than our previous generations. Enhancements also include full out-of-order processing, non-blocking high-throughput L1 caches, and advanced instruction and data prefetching.



Cortex-A76AE Overview

Arm Cortex-A76AE brings highest levels of safety with Split-Lock capability which includes the ability for Dual Core Lock-Step (DCLS). Cortex-A76AE also delivers uncompromising performance and thermal efficiency. It is the processor of choice for next generation Advanced Driver-Assistance Systems (ADAS) and Autonomous Driving systems.

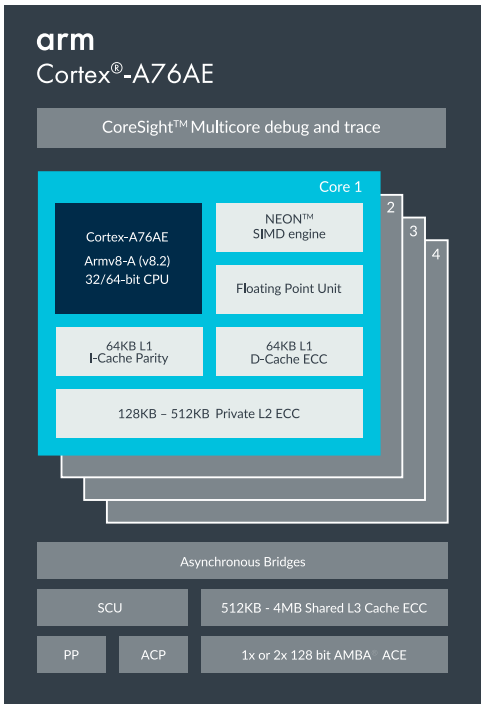
Key Features Compared to Cortex-A75:

- **35%** improved performance per core
- **40%** better power efficiency per core

Safety Ready

Arm Cortex-A76AE is part of Arm's Safety Ready portfolio, a collection of Arm IP that have been through various and rigorous levels of functional safety systematic flows and development.

Learn more at www.arm.com/safety



Specifications

Architecture	Armv8-A (Harvard)	
Extensions	• Armv8.1 extensions • Armv8.2 extensions • Cryptography extensions • RAS extensions • Armv8.3 (LDAPR instructions only) • Armv8.4 Dot Product	
ISA support	• A64 • A32 and T32 (at the EL0 only)	
Microarchitecture	Pipeline	Out-of-order
	Superscalar	Yes
	Neon / Floating Point Unit	Included
	Cryptography Unit	Optional
	Max number of CPUs in cluster	Four (4)
	Physical Addressing (PA)	40-bit
Memory system and external interfaces	L1 I-Cache / D-Cache	64KB
	L2 Cache	128KB to 512KB
	L3 Cache	Optional, 512KB to 4MB
	ECC Support	Yes
	LPAE	Yes
	Bus interfaces	AMBA ACE or CHI
	ACP	Optional
	Peripheral Port	Optional
Functional safety	Dual Core Lock-Step	Yes (in Lock-mode)
	Memory protection	Yes
	Interface protection	Yes
	Safety capability	• Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D systematic development
	Safety Package	Yes (Extended Package)
Other	Security	TrustZone
	Interrupts	GIC interface, GICv4
	Generic timer	Armv8-A
	PMU	PMUv3
	Debug	Armv8-A (plus Armv8.2-A extensions)
	CoreSight	CoreSightv3
	Embedded Trace Macrocell	ETMv4.2 (instruction trace)

Related Products

Cortex-A65AE

High throughput efficiency Automotive Enhanced Cortex-A CPU for high-end autonomous systems targeting up to ASIL D.

CoreLink CMN-600AE

Designed for high performance automotive systems across a wide range of applications.

CoreLink GIC-600AE

Software compatible with GIC-600. Additional features meet safety requirements for building high-performance ASIL B to ASIL D systems.

Arm Compiler

Arm Compiler 6 has been certified by safety experts TÜV SÜD as fulfilling the requirements for development tools classified as T3 according to safety standard IEC 61508.

CoreLink MMU-600AE

Software compatible with MMU-600. Adds additional safety features to meet safety requirements for building high-performance ASIL B to ASIL D systems.