Benefits

1. Thermal Efficiency

Contains the latest state-of-the-art microarchitecture features that deliver greater single-thread integer, floating-point, memory and ML performance. Executes workloads with sustained performance within constrained power envelopes.

2. Flexibility with Split-Lock

Switch between split mode for highest multicore performance or lock mode for advanced multicore fault-tolerance with ASIL D hardware metrics.

Provide additional flexibility for future mixed-criticality applications.

3. Superscalar Processor Core

The superscalar processor core decodes, issues, and executes more instructions than our previous generations. Enhancements also include full out-of-order processing, non-blocking high-throughput L1 caches, and advanced instruction and data prefetching.

Cortex-A76AE Overview

Arm Cortex-A76AE brings highest levels of safety with Split-Lock capability which includes the ability for Dual Core Lock-Step (DCLS). Cortex-A76AE also delivers uncompromising performance and thermal efficiency. It is the processor of choice for next generation Advanced Driver-Assistance Systems (ADAS) and Autonomous Driving systems.

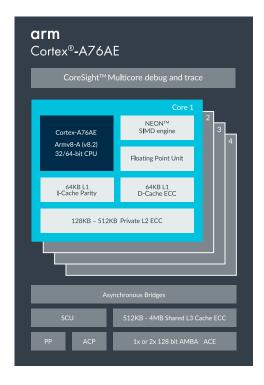
Key Features Compared to Cortex-A75:

- → 35% improved performance per core



Arm Cortex-A76AE is part of Arm's Safety Ready portfolio, a collection of Arm IP that have been through various and rigorous levels of functional safety systematic flows and development.

Learn more at www.arm.com/safety





Specifications

Extensions	Architecture	Armv8-A (Harvard)	
• A32 and T32 (at the ELO only) Microarchitecture Pipeline Superscalar Neon / Floating Point Unit Included Cryptography Unit Optional Max number of CPUs in cluster Physical Addressing (PA) Memory system and external interfaces L1 I-Cache / D-Cache L2 Cache L3 Cache C2 Support L9AE Ves Bus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Peripheral Port Dual Core Lock-Step Memory yes Interface protection Yes Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D	Extensions	 Armv8.2 extensions Cryptography extensions RAS extensions Armv8.3 (LDAPR instructions only) 	
Superscalar Neon / Floating Point Unit Included Cryptography Unit Optional Max number of CPUs in cluster Physical Addressing (PA) 40-bit Memory system and external interfaces L1 I-Cache / D-Cache 64KB L2 Cache L3 Cache D9tional, 512KB to 512KB L3 Cache Optional, 512KB to 4MB ECC Support Yes LPAE Yes Bus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Functional safety Dual Core Lock-Step Memory protection Yes Interface protection Yes Safety capability - Contributes towards up to ASIL D hardware diagnostic metrics Supposed to the suppos	ISA support		
Neon / Floating Point Unit Included Cryptography Unit Optional Max number of CPUs in cluster Four (4) Physical Addressing (PA) 40-bit Memory system and external interfaces L1 I-Cache / D-Cache 64KB L2 Cache 128KB to 512KB L3 Cache Optional, 512KB to 4MB ECC Support Yes LPAE Yes Bus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Functional safety Dual Core Lock-Step Yes (in Lock-mode) Memory protection Yes Interface protection Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D	Microarchitecture	Pipeline	Out-of-order
Cryptography Unit Max number of CPUs in cluster Pour (4) Physical Addressing (PA) L1 I-Cache / D-Cache L2 Cache L3 Cache L3 Cache CCS Support LPAE Bus interfaces AMBA ACE or CHI ACP Peripheral Port Dual Core Lock-Step Memory protection Interface protection Safety capability Cryptography Unit Pour (4) Four		Superscalar	Yes
Max number of CPUs in cluster Physical Addressing (PA) 40-bit Memory system and external interfaces L1 I-Cache / D-Cache 64KB L2 Cache L3 Cache C9tional, 512KB to 4MB ECC Support Yes LPAE Sus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Functional safety Dual Core Lock-Step Memory protection Interface protection Safety capability Functional safety Four (4) 40-bit Four (4) 40-bit 40-b		Neon / Floating Point Unit	Included
Physical Addressing (PA) Memory system and external interfaces L1 I-Cache / D-Cache L2 Cache L3 Cache L3 Cache Optional, 512KB to 512KB CCC Support Yes LPAE Bus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Functional safety Dual Core Lock-Step Memory protection Yes Interface protection Yes Safety capability Contributes towards up to ASIL D hardware diagnostic metrics Suitable for up to ASIL D		Cryptography Unit	Optional
Memory system and external interfaces L1 I-Cache / D-Cache 64KB L2 Cache 128KB to 512KB L3 Cache Optional, 512KB to 4MB ECC Support Yes LPAE Yes Bus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Functional safety Dual Core Lock-Step Yes (in Lock-mode) Memory protection Yes Interface protection Yes Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D		Max number of CPUs in cluster	Four (4)
L2 Cache L3 Cache Optional, 512KB to 4MB ECC Support Yes LPAE Sus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Peripheral Port Optional Functional safety Dual Core Lock-Step Memory protection Memory protection Yes Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D		Physical Addressing (PA)	40-bit
L3 Cache ECC Support Yes LPAE Bus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Functional safety Dual Core Lock-Step Memory protection Interface protection Safety capability Contributes towards up to ASIL D hardware diagnostic metrics Suitable for up to ASIL D	Memory system and external interfaces	L1 I-Cache / D-Cache	64KB
ECC Support LPAE Sus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Functional safety Dual Core Lock-Step Yes (in Lock-mode) Memory protection Yes Interface protection Yes Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D		L2 Cache	128KB to 512KB
LPAE Bus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Functional safety Dual Core Lock-Step Memory protection Interface protection Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D		L3 Cache	Optional, 512KB to 4MB
Bus interfaces AMBA ACE or CHI ACP Optional Peripheral Port Optional Yes (in Lock-mode) Memory protection Interface protection Yes Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D		ECC Support	Yes
ACP Optional Peripheral Port Optional Functional safety Dual Core Lock-Step Yes (in Lock-mode) Memory protection Yes Interface protection Yes Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D		LPAE	Yes
Peripheral Port Optional Functional safety Dual Core Lock-Step Yes (in Lock-mode) Memory protection Yes Interface protection Yes Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D		Bus interfaces	AMBA ACE or CHI
Functional safety Dual Core Lock-Step Yes (in Lock-mode) Memory protection Yes Interface protection Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D		ACP	Optional
Memory protection Interface protection Yes Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D		Peripheral Port	Optional
Interface protection Safety capability • Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D	Functional safety	Dual Core Lock-Step	Yes (in Lock-mode)
 Safety capability Contributes towards up to ASIL D hardware diagnostic metrics Suitable for up to ASIL D 		Memory protection	Yes
hardware diagnostic metrics • Suitable for up to ASIL D		Interface protection	Yes
systematic development		Safety capability	hardware diagnostic metrics
Safety Package Yes (Extended Package)		Safety Package	Yes (Extended Package)
Other Security TrustZone	Other	Security	TrustZone
Interrupts GIC interface, GICv4		Interrupts	GIC interface, GICv4
Generic timer Armv8-A		Generic timer	Armv8-A
PMU PMUv3		PMU	PMUv3
Debug Armv8-A (plus Armv8.2-A extensions)		Debug	Armv8-A (plus Armv8.2-A extensions)
CoreSight CoreSightv3		CoreSight	CoreSightv3
Embedded Trace Macrocell ETMv4.2 (instruction trace)		Embedded Trace Macrocell	ETMv4.2 (instruction trace)

Related Products

Cortex-A65AE

High throughput efficiency Automotive Enhanced Cortex-A CPU for high-end autonomous systems targeting up to ASIL D.

CoreLink CMN-600AE

Designed for high performance automotive systems across a wide range of applications.

CoreLink GIC-600AE

Software compatible with GIC-600. Additional features meet safety requirements for building high-performance ASIL B to ASIL D systems.

Arm Compiler

Arm Compiler 6 has been certified by safety experts TÜV SÜD as fulfilling the requirements for development tools classified as T3 according to safety standard IEC 61508.

CoreLink MMU-600AE

Software compatible with MMU-600. Adds additional safety features to meet safety requirements for building high-performance ASIL B to ASIL D systems.