Arm Cortex-M55 Processor

arm

Product Brief

KEY FEATURES AND BENEFITS

- **Enhanced endpoint AI performance**
  The first processor based on Arm Helium technology with the highest, most efficient ML and DSP performance for Cortex-M
- **Flexibility to differentiate**
  Arm Custom Instructions extends the processor's capabilities for workload-specific optimization
- **Faster time to market**
  The Corstone-300 reference design offers the fastest, most secure way to incorporate the Cortex-M55 into an SoC
- **Simplified software development**
  Integrated into a single developer toolchain supported by a broad ecosystem of software, tools, libraries and resources

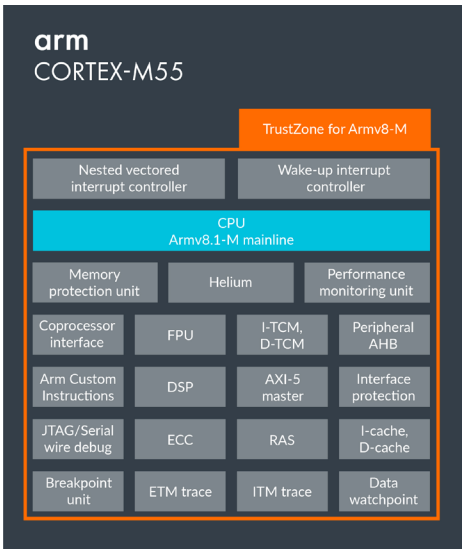

Fig.1
Arm Cortex-M55 processor block diagram

Most AI-Capable Cortex-M Processor

Introduction

The Arm Cortex-M55 processor brings the benefits of endpoint AI to billions more devices and empowers developers to deliver the next revolution in computing. It is Arm's most AI-capable Cortex-M processor and the first to feature Arm Helium vector processing technology, bringing enhanced, power-efficient DSP and ML performance. Cortex-M55 offers an easy way to implement AI for a wide range of IoT use cases with the ease of use of Cortex-M, a single toolchain, optimized software libraries, and an industry-leading embedded ecosystem.

Highlights

Arm Helium Technology

Helium* is a new vector instruction set extension in the Armv8.1-M architecture that enables a significant uplift in DSP and ML capabilities. The vector processing extension adds over 150 new scalar and vector instructions, enabling the efficient compute of 8-bit, 16-bit, and 32-bit fixed point data. 16-bit and 32-bit fixed point formats are used in traditional signal processing applications, such as audio processing. The 8-bit fixed point format can be important to ML processing. Helium vector processing technology allows arithmetic operations to occur simultaneously, improving throughput and maximizing the use of processor resources. As an example, the table below shows the throughput per cycle that can be achieved when executing a multiply-accumulate operation.

Datatype	8-bit integer	16-bit integer	32-bit integer	Half-precision floating-point	Single-precision floating-point
MACs/ cycle	8	4	2	4	2

Floating-point Unit

The Cortex-M55 Floating-point Unit (FPU)* natively supports vector and scalar half-precision and single-precision floating-point datatypes. Additionally, the FPU provides native support for scalar double-precision floating-point calculations. The half-precision floating-point processes twice the amount of data per clock cycle when compared to using single-precision floats, reducing the memory footprint of data storage. This is ideal for applications with sound and sensor data processing where the resolution of the data is low, but still needs a high dynamic range.

Security

Arm TrustZone technology* is supported in the Cortex-M55 processor, reducing the potential for software-based attacks by isolating the critical information from the rest of the application. Armv8.1-M introduces several security enhancements, including a new Memory Protection Unit (MPU) region attribute called Privileged eXecute Never (PXN), the Unprivileged Debug Extension (UDE), and some additional TrustZone enhancements that offer isolated debug permissions of different software components in each security domain of the processor. All these features enhance security and accelerate the route to PSA Certified silicon and devices.

Arm Custom Instructions

Arm Custom Instructions* enable designers to push the performance and efficiency of the processor further by adding application domain-specific features, while maintaining all the advantages of Arm's software ecosystem. They allow developers to add a customizable module inside the Cortex-M55 processor. This module is driven by the pre-decoded instructions and shares the same interface as the standard Arithmetic Logic Unit (ALU) of the processor. *(Arm Custom Instructions will be available in the Cortex-M55 in 2021).*

Coprocessor Interface

The coprocessor interface* opens the door for customization and extensibility to further decrease the power consumption of the system in the presence of frequent compute-intensive operations. Even though this feature is not new to Cortex-M, it is an important feature that allows system-on-chip (SoC) designers to create closely coupled hardware accelerators to speed up a range of processing functions.

Debug Feature Enhancements

The Cortex-M55 processor features new debug enhancements, including the Performance Monitoring Unit (PMU) with eight 16-bit event counters, direct cache access registers that allow the cache states to be accessed, and the Unprivileged Debug Extension (UDE) that restricts debug visibility to a specific software partition.

Arm Corstone-300 Reference Design

Corstone-300* is the ultimate starting point for integrating the Cortex-M55 processor into an SoC with the lowest risk and development cost. The Corstone-300 reference design integrates the processor, security components such as SIE-300 AXI5 TrustZone controllers, and system IP such as Power Control Kit PCK-600. It is well supported by open-source software including Trusted Firmware-M and development tools. The Corstone-300 simplifies security implementation with an optimized AXI5 system for Arm TrustZone technology, accelerating the route to PSA Certified silicon and devices.

Arm Ethos-U55 microNPU

Ethos-U55* is the industry's first microNPU designed for microcontroller-class devices. It is integrated with a single Cortex-M toolchain to provide exceptional performance uplift without additional software complexity. Combining the Cortex-M55 processor with Ethos-U55 can deliver up to a 480x uplift in ML performance over previous-generation Cortex-M processors.

Software and Tools

The Cortex-M55 processor improves the efficiency of AI development on endpoint devices. Developers can take advantage of the ease-of-use of Cortex-M, a single toolchain, optimized software libraries and frameworks, such as TensorFlow Micro, and an industry-leading embedded ecosystem. All are supported by an extensive knowledge base and set of resources to make software development for the Cortex-M55 processor as fast and easy as possible.

Specifications

Key Features	Architecture	Armv8.1-M
	Bus Interface	AMBA 5 AXI5 64-bit master (compatible to AXI4 IPs)
	Pipeline	4-stage
	Security	TrustZone technology*
	DSP Extension	32-bit DSP/SIMD extension
	M-profile Vector Extension	Helium*
	Floating-Point Unit	FPU*
	Coprocessor Interface	64-bit*
	Innovation	Arm Custom Instructions*
Memory System	Instruction Cache	Up to 64KB with ECC*
	Data Cache	Up to 64KB with ECC*
	Instruction TCM	Up to 16MB with ECC*
	Data TCM	Up to 16MB with ECC*
	Interrupts	Up to 480 interrupts + Non-maskable interrupt (NMI)
	Wake-up Interrupt Controller	Internal and/or external*
	Sleep modes	Multiple power domains, sleep modes (sleep and deep sleep), sleep-on-exit, optional retention support for memories and logic
Development Platform	Debug	Hardware and software breakpoints Performance Monitoring Unit (PMU)
	Trace	Optional Instruction Trace Data Trace (DWT) (selective data trace, profiling and event trace) Instrumentation Trace (ITM) (software trace)
	Software	CMSIS - CMSIS-DSP and CMSIS-NN Pelion IoT Platform Mbed OS Trusted Firmware-M ML frameworks, such as TensorFlow Lite Micro
	Tools	Arm Development Studio Arm Keil MDK Software Development Tool Cortex-M Prototyping System Fast Models and Fixed Virtual Platform

Use Cases

The Cortex-M55 processor with Helium technology opens up opportunities in new market segments across a wider range of use cases. The Cortex-M55 is designed to enhance the following use cases:

Earbuds

Fingerprint unlock

Health trackers

Predictive maintenance

Smart speakers

Video doorbell

Learn more about the Cortex-M55 processor and supporting IP in this white paper or contact an Arm expert for more details.

**Optional features of the Cortex-M55 processor*

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