Cortex-A65AE

Automotive Enhanced

Datasheet

Benefits

1. **Simultaneous Multithreading**

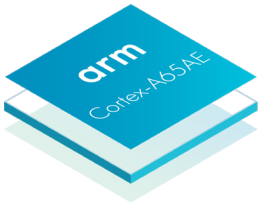
   The multithreaded processor, a first in the Cortex family, has an out-of-order execution pipeline and can execute two-threads in parallel on each cycle. Each thread can be at different exception levels and run different operating systems.

2. **Flexibility with Split-Lock**

   Switch between split mode for highest multicore performance or lock mode for advanced multicore fault-tolerance with ASIL D hardware metrics. Provide additional flexibility for future mixed-criticality applications.

3. **Throughput Efficiency**

   The Cortex-A65AE features an advanced microarchitecture designed for performance density and delivers high-throughput efficiency for memory intensive workloads in constrained thermal budgets.



Cortex-A65AE Overview

The Cortex-A65AE is the first multithreaded Cortex-A CPU for automotive applications and safety critical tasks such as Advanced Driver-Assistance Systems (ADAS) and Gateway. It is designed for devices undertaking high throughput and safety critical tasks. The Cortex-A65AE is built on DynamIQ technology and benefits from its resilience and flexible multicore features. It has also been designed with Dual Core Lock-Step (DCLS), an advanced feature for increased fault-tolerance designs.

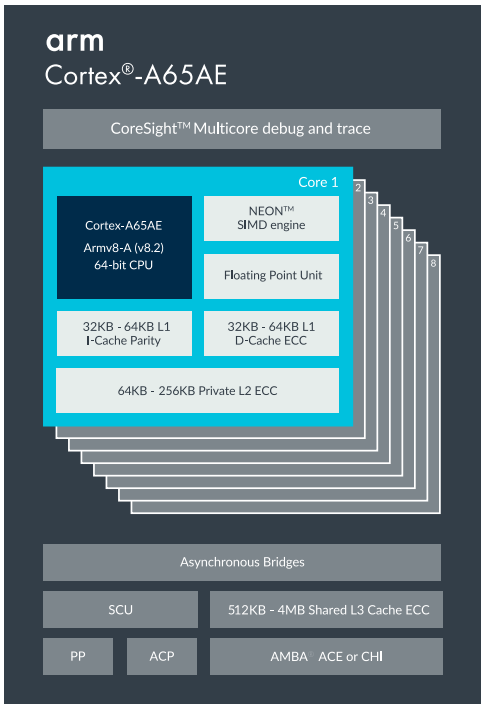
Key Benefits Compared to Cortex-A53 (at iso-frequency):

- **80%** higher integer performance per core
- **3.5x** higher memory throughput for memory intensive automotive workloads
- **6x** higher Machine Learning performance
- **>6x** higher read bandwidth through a low-latency co-processing interface for closely-coupled accelerators

Safety Ready

Arm Cortex-A65AE is part of Arm's Safety Ready portfolio, a collection of Arm IP that has been through various and rigorous levels of functional safety systematic flows and development.

Learn more at www.arm.com/safety



Specifications

Architecture	Armv8-A (Harvard)	
Extensions	• Armv8.1 extensions • Armv8.2 extensions • Cryptography extensions • RAS extensions • Armv8.3 (LDAPR instructions only) • Armv8.4 Dot Product	
ISA support	• A64	
Microarchitecture	Pipeline	Out-of-order
	Superscalar	Yes
	Neon / Floating Point Unit	Included
	Cryptography Unit	Optional
	Max number of CPUs in cluster	Eight (8)
	Physical Addressing (PA)	44-bit
Memory system and external interfaces	L1 I-Cache / D-Cache	32KB to 64KB
	L2 Cache	64KB to 256KB
	L3 Cache	Optional, 512KB to 4MB
	ECC Support	Yes
	LPAE	Yes
	Bus interfaces	AMBA ACE or CHI
	ACP	Optional
	Peripheral Port	Optional
Functional safety	Dual Core Lock-Step	Yes (in Lock-mode)
	Memory protection	Yes
	Interface protection	Yes
	Safety capability	• Contributes towards up to ASIL D hardware diagnostic metrics • Suitable for up to ASIL D systematic development
	Safety Package	Yes (Extended Package)
Other	Security	TrustZone
	Interrupts	GIC interface, GICv4
	Generic timer	Armv8-A
	PMU	PMUv3
	Debug	Armv8-A (plus Armv8.2-A extensions)
	CoreSight	CoreSightv3
	Embedded Trace Macrocell	ETMv4.2 (instruction trace)

Related Products

Cortex-A76AE

High performance Automotive Enhanced Cortex-A CPU for high-end autonomous systems targeting up to ASIL D.

CoreLink CMN-600AE

Designed for high performance automotive systems across a wide range of applications.

CoreLink GIC-600AE

Software compatible with GIC-600. Additional features meet safety requirements for building high-performance ASIL B to ASIL D systems.

Arm Compiler

Arm Compiler 6 has been certified by safety experts TÜV SÜD as fulfilling the requirements for development tools classified as T3 according to safety standard IEC 61508.

CoreLink MMU-600AE

Software compatible with MMU-600. Adds additional safety features to meet safety requirements for building high-performance ASIL B to ASIL D systems.