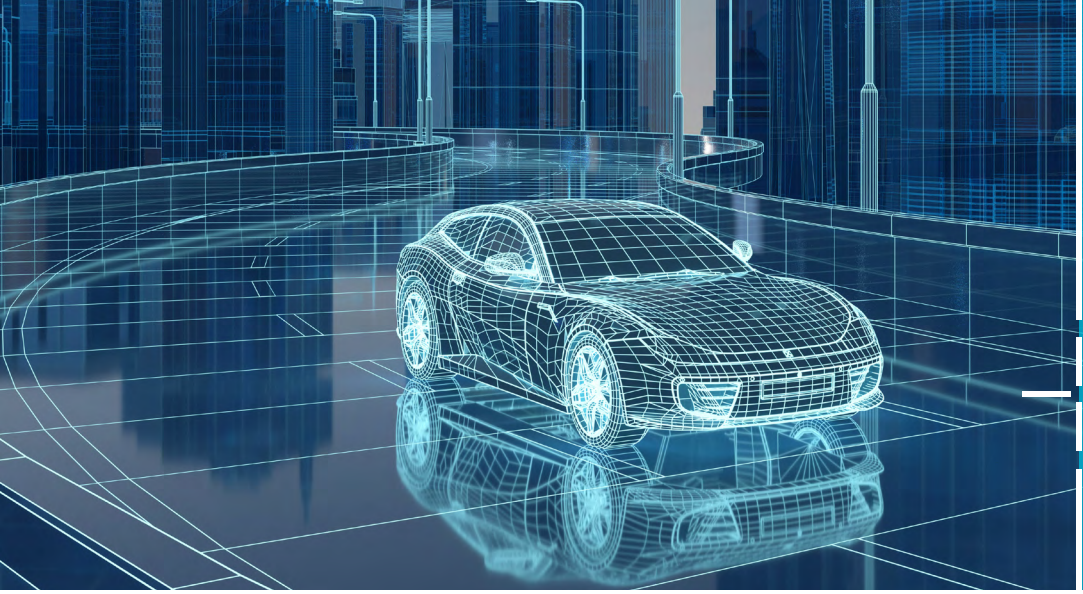


PRODUCT BRIEF

Arm Cortex-A520AE CPU

KEY FEATURES AND BENEFITS

- Leading Power Efficiency with Significant Performance Uplift
  Cortex-A520AE CPU is designed to achieve leading power efficiency with a performance uplift of 30 percent compared to the highly adopted Cortex-A55.
- Scalability Across Automotive Applications
  Cortex-A520AE can be used in scalable CPU cluster configurations to suit digital cockpit, ADAS, and zonal controller use cases.
- Additional Functional Safety features
  Cortex-A520AE adds functional safety capabilities for advanced safety requirements in the modern software-defined vehicle (SDV).

INTRODUCTION

Across all vehicles, there is a greater demand for more advanced computing capabilities to enable the seamless experiences and driver assistance features that users have come to expect through new AI-accelerated SDVs.

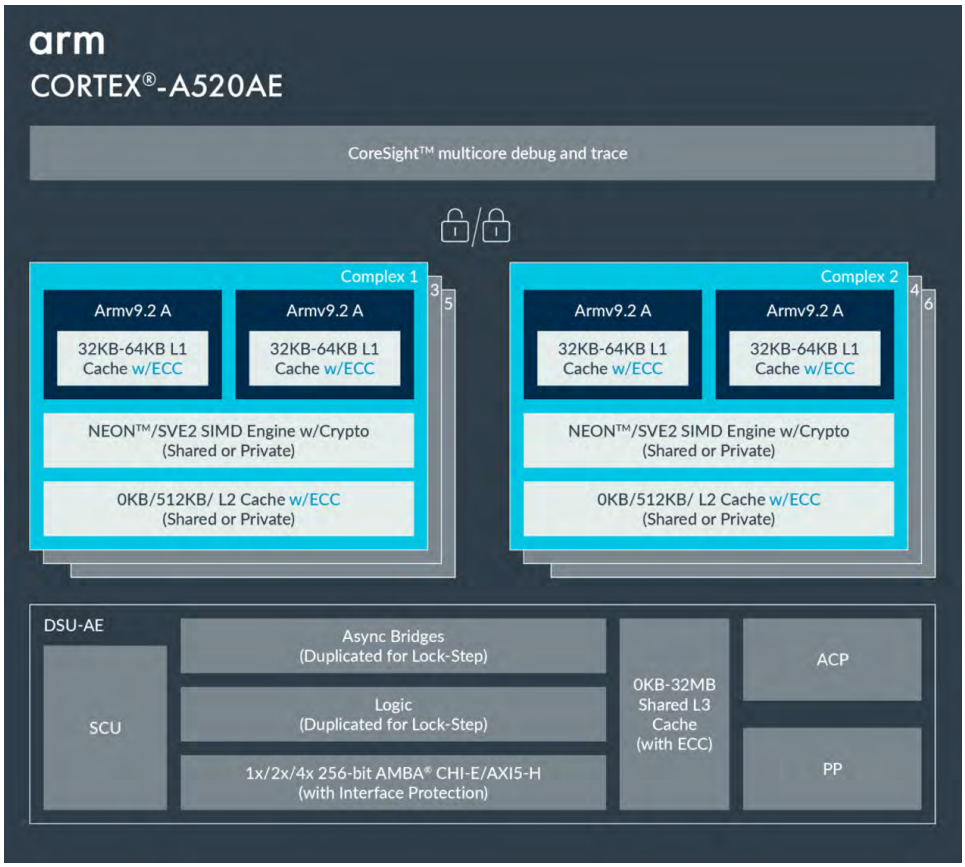
Leveraging the success of the Arm Cortex-A CPUs for consumer devices, the Arm Automotive Enhanced (AE) variant of the A-class series of CPUs have seen broad adoption across a wide range of automotive applications. These include:

- ADAS
- Digital cockpits, including both IVI systems and instrument clusters
- Vehicle domain controllers
- Central computers

USE CASES

- Digital Cockpit
- In-Vehicle Infotainment (IVI)
- Advanced Driver-Assistance Systems (ADAS)
- Zonal Controllers

Key aspects across all these applications are more advanced functional safety and security features that ensure road safety for drivers, passengers, and pedestrians, as well as securing driver and vehicle data.



HIGHLIGHTS

Industry-Leading Scalable Power Efficiency

Cortex-A520AE is our latest high-efficiency Cortex-A processor targeted at safety-critical, automotive use-cases. It has been designed to achieve leading power efficiency, while still bringing a performance uplift of 30 percent compared to the highly adopted Arm Cortex-A55.[1] It is the first Arm Cortex-A AE CPU to introduce the merged-core micro-architecture, enabling power and performance gains to be achieved in a low silicon area. Highly configurable and compatible with Arm DSU-120AE, Cortex-A520AE can be used in scalable CPU cluster configurations to suit digital cockpit, ADAS, and zonal controller use cases.

More Functional Safety Capabilities

Cortex-A520AE adds further functional safety capabilities on top of what was offered by Cortex-A55 and Arm Cortex-A65AE CPUs. These enable new, efficient ways for system integrators to deliver on the varying safety requirements across the SDV. The widely adopted split-lock feature, which enables the ability to boot the cluster in Split, Hybrid, or Lock modes, has been maintained and extended to bring even more flexibility. This enables SoC designers to create a single product that can be deployed in systems with different safety integrity requirements.

Meanwhile, the introduction of the Transient Fault Protection (TFP) configuration option augments the diagnostic fault coverage provided by Hybrid-mode, Arm Software Test Libraries, and memory and interface protection to target ASIL B safety levels. These features – that are also built into Arm Cortex-A720AE – have been designed to work together in safety-critical applications that require even greater levels of performance scalability.

Advanced Security and AI Features through Armv9.2 A Architecture

Cortex-A520AE is built on the Armv9.2 A architecture, enabling new features around security, AI performance, and quality of service (QoS).

Security enhancements include Pointer Authentication (PAC), Branch Target Identification (BTI) and Memory Tagging Extension (MTE) features that remove up to 95 percent of certain classes of vulnerabilities, including memory safety violations that account for the majority of all serious security bugs. MTE allows developers to detect and avoid memory safety vulnerabilities before and after deployment, helping to speed up the application debugging and development process.

Many new architectural features have been designed to enhance AI performance, including support for new data types, such as BFloat16, as well as support for Matrix Multiply, and the introduction of Scalable Vector Extensions (SVE2), an evolution of the Arm NEON SIMD engine.

FOOTNOTES

[1] Comparing Arm Cortex-A520 and Cortex-A55 SPECrate2017_int performance in iso-configuration, iso-process, and at iso-frequency.