Arm Cortex-R52

Product Brief

Benefits

1. Software Separation

Robust hardware-enforced software separation provides confidence that software functions can't interfere with each other. For safety-related tasks, this can mean less code needs to be certified, saving time, cost and effort.

2. Multiple OS Support

Virtualization support gives developers flexibility, readily allowing consolidation of applications using multiple operating systems within a single CPU. This eases the addition of functionality without growing the number of electronic control units.

3. Real-Time Performance

High-performance multicore clusters of Cortex-R52 CPUs deliver real-time responsiveness for deterministic systems with the lowest Cortex-R latency.

Overview

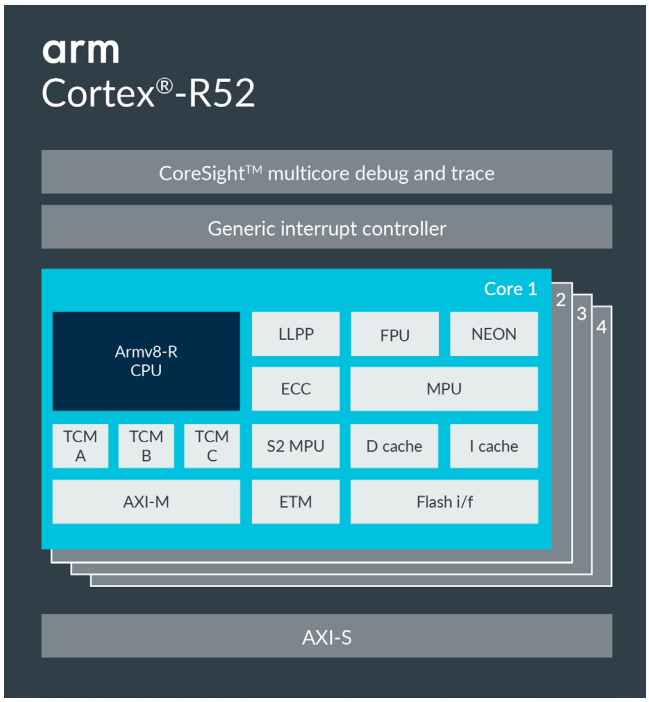
The Cortex-R52 is the most advanced processor in the Cortex-R family delivering real-time performance for functional safety. As the first Armv8-R processor, Cortex-R52 introduces support for a hypervisor, simplifying software integration with robust separation to protect safety-critical code, while maintaining real-time deterministic operation required in high dependable control systems.

Cortex-R52 addresses a range of applications such as high performance domain controllers for vehicle powertrain and chassis systems or as a safety island providing protection in complex ADAS and Autonomous Drive systems.

Safety Ready

Arm Cortex-R52 is part of Arm's Safety Ready portfolio, a collection of Arm IP that have been through various and rigorous levels of functional safety systematic flows and development.

Learn more at www.arm.com/safety



Specifications

Architecture	Armv8-R
Instruction Set	Arm and Thumb-2. Supports DSP instructions and a configurable Floating-Point Unit either with single-precision or double precision and Neon.
Microarchitecture	8-stage pipeline with superscalar in order execution and branch prediction. Binary compatible with the Arm9, Arm11, Cortex-R4, Cortex-R5, Cortex-R7 and Cortex-R8 embedded processors.
Up to quad-core	Multi-processor configurations of up to 4 integer CPUs within a single cluster or 8 logical cores (in DCLS configuration), within a single cluster all of which can have a lockstep copy.
Dual Core Lock Step (DCLS)	Redundant Cortex-R52 cores in lockstep for fault detection in dependable systems with optional flexibility through split/lock configuration to decouple checking core enabling independent execution.
Safety Package	Licensable, extended safety package to simplify product safety implementation.
Self Test Technology	Fault coverage through 'Built In Self Test' capabilities (BIST).
Software Test Libraries	Licensable library of software tests which can be called and flexibly executed during run time offering non-destructive fault coverage of the processors logic.
Cache controllers	Optional Harvard memory architecture with write through Intruction and Data cache. Cache sizes are independently configurable for 4K to 32K.
Tightly-Coupled Memories	Optional Tightly Coupled Memory available for deterministic or low-latency applications such as interrupt service routines or frequently used data. Up to 3 flexibly configurable TCMs memories each up to 1Mbyte.
Generic Interrupt Controller	Fully integrated Generic Interrupt Controller (GIC). Configurable to support from 32 to 960 interrupts with priority-based interrupt handling.
Memory Protection Unit (MPU)	Two stage MPUs interdependently configurable to support 24 regions from 64 bytes upwards. Enabling real time virtualization.
Floating-Point Unit (FPU)	Single or double precision Floating Point Unit with up to 32 64 bit or 16 128 bit double precision registers.
Advanced SIMD (NEON)	Optionally implement when double precision floating point is included is the Advanced SIMD supporting integer or single precision results.
ECC	Single-bit error correction and double-bit error detection for cache and TCM memories with hard error protection. All bus interfaces protected using Error Correcting Code (ECC).
Bus Interconnect Protection	Optional additional protection to guard against errors in the interconnect switch fabric, and end to transaction protection.
Master AMBA AXI bus	128-bit AMBA AXI-4 bus master for Level-2 memory and peripheral access, with ECC protection.
Slave bus	128-bit slave port allows DMA masters to access the TCMs for high speed streaming of data in and out of the processor, with ECC protection.
Low Latency Peripheral Port (LLPP)	A shared dedicated 32-bit AMBA AXI port to integrate latency-sensitive peripherals more tightly with the processor, with ECC protection.
Flash Interface Port	Per core dedicated 128-bit AMBA AXI port to integrate latency-sensitive Flash memory tightly to a specific core within the processor cluster, ECC protection configurable for either 128-bit or 64-bit chunk size.
Debug	Debug Access Port is provided. Its functionality can be extended using CoreSight Debug and Trace.
Trace	Cortex-R52 includes a CoreSight Embedded Trace Module that can be configured per core or shared between the cores in the cluster.

Related Products

Safety Documentary Package

Arm's Safety Documentation Package for Cortex-R52 provides information for partners implementing safety related features. It includes comprehensive details on specific product safety features, verification and Failure Mode Effects & Diagnostic Analysis (FMEDA). The Safety Documentation package simplifies integration of the Cortex-R52 into in systems with ISO 26262 and IEC 61508 requirements.

Software Test Libraries

Arm's Software Test Libraries provide diagnostic coverage to address functional safety requirements for ISO 26262 and IEC 61509 systems with flexible execution scheduling minimizing the run time impact on the application.

Fast Models

Fast Models are accurate, flexible programmer's view models of Arm IP, allowing the development of software such as drivers, firmware, Operating Systems and applications which can be widely deployed independently to silicon availability.

Cycle Models

Cycle Models are cycle accurate, flexible models of Arm IP, allowing you to precisely model software performance such as drivers and firmware prior to silicon availability.

Development Boards

Arm Versatile Express development boards are the ideal platform for accelerating the development and reducing the risk of new SoC designs. Evaluate, benchmark, prototype drivers, and test custom logic blocks or system IP. Image available for Cortex-R52 subsystem for use on the Arm MPS3 FPGA prototyping board.

Arm Developer Studio

One professional package equipping engineering teams to bring products to market faster and cost effectively. Combining the best of Arm and Keil development tools and middleware, Development Studio seamlessly covers the entire product lifecycle, from SoC architecture exploration to software integration and testing. A safety certified version of the tool is also available including qualification kit and documentation.

CoreSight Debug and Trace

Arm offers a portfolio of IP to support debug features to observe or modify the state of parts of the design, while trace features allow continuous collection of system information. System developers can select the most appropriate CoreSight components based on their system requirements.