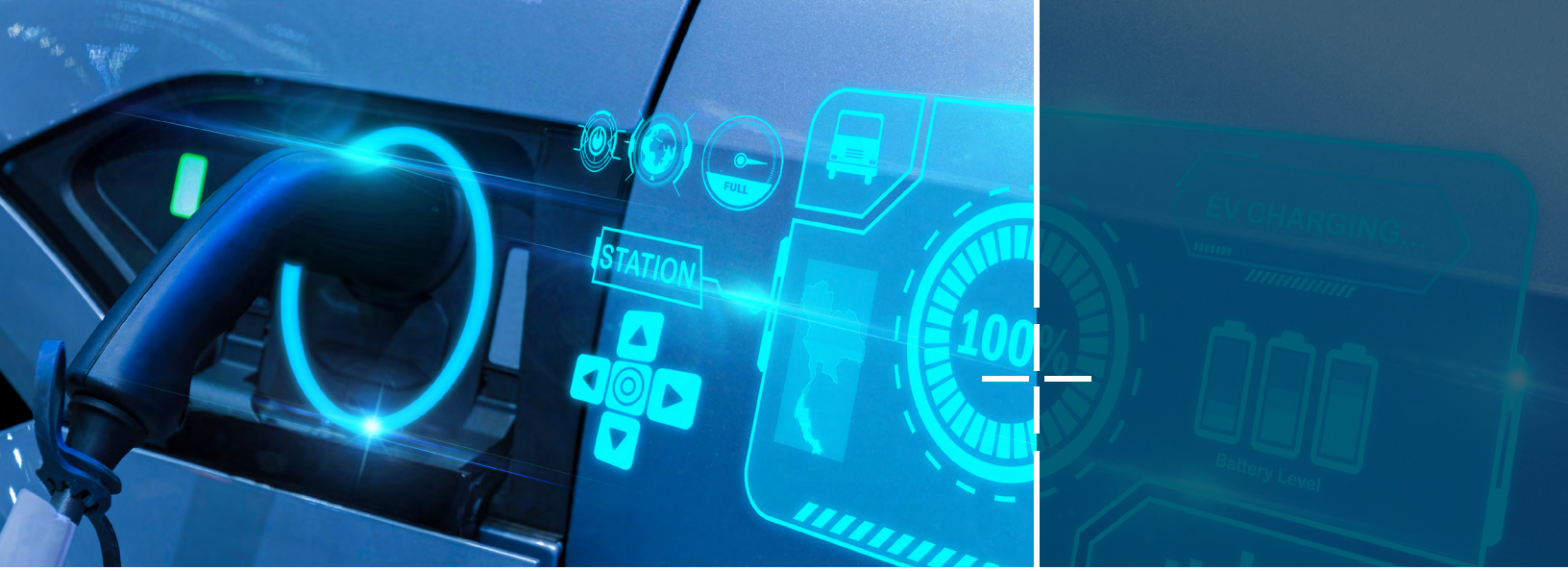
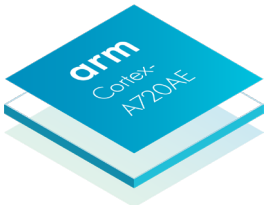


PRODUCT BRIEF

Arm Cortex-A720AE



KEY FEATURES AND BENEFITS

- Industry-Leading Functional Safety
  Includes safety features that target ASIL D and ASIL B ISO 26262 Hardware Diagnostic Certification as a Safety Elements Out of Context (SEooC). Combines optional Arm Software Test Library and Transient Fault Protection, and AMBA interface protection on all external interfaces, with split-lock technology for use in a broad range of safety applications
- Performance Scalability
  The new Arm DynamIQ Shared Unit-120AE (DSU-120AE) vastly increases performance scalability and system-on-chip (SoC) design flexibility, with support for up to 14 CPUs in a single CPU cluster, and multiple clusters that can be supported with CMN S3AE.

INTRODUCTION

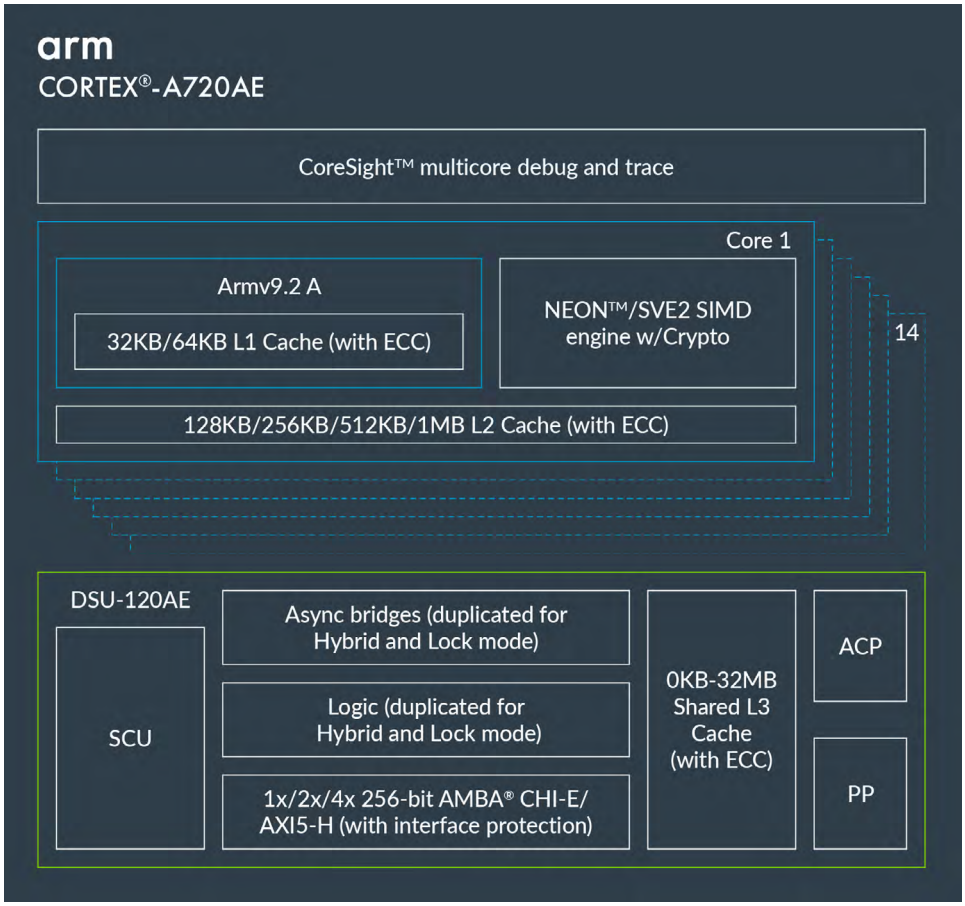
The Arm Cortex-A720AE CPU enables Armv9-A computing capabilities and is integrated with the new Arm DynamIQ Shared Unit, DSU-120AE, which provides intelligent power-saving features, enhanced PPA and improved scalability. This enables the CPU clusters featuring Cortex-A720AE to reach high levels of performance and efficiency, while delivering new functional safety features targeted at certifications as an SEooC, with flexibility to address ASIL D and ASIL B, as well as Quality Management (QM) use cases.

DSU-120AE also provides support for heterogeneous designs with the Arm Cortex-A520AE for the combination of performance and efficiency CPUs within a single cluster.

- First Armv9-A Automotive Enhanced CPU
  System developers benefit from the latest Armv9.2A features, which provide security, AI processing, software portability and virtualization improvements. These are all delivered at improved power and similar area efficiency to the Armv8.2A Cortex-A78AE.[1]

USE CASES

- Digital Cockpit
- In-Vehicle-Infotainment (IVI)
- Advanced Driver-Assistance Systems (ADAS)
- Vehicle Central Compute



HIGHLIGHTS

Industry-Leading Functional Safety

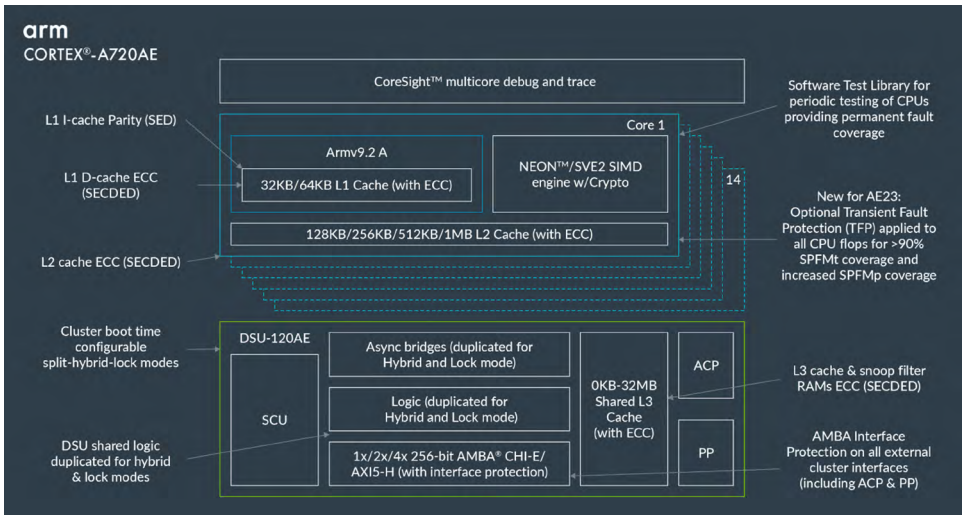
The Arm Cortex-A720AE is the industry-leading IP for sustained premium performance in safety-critical use cases. It delivers a 1.2x performance uplift relative to Cortex-A78AE[2] and configurable functional safety features that make it suitable for use in quality-managed, and ISO 26262 ASIL B and ASIL D systems, which include:

- Cluster boot-time configurable split, hybrid, or lock modes targeted at QM, ASIL B, and ASIL D use cases respectively;
- Optional Arm Software Test Library (STL) that provides permanent fault diagnostic coverage while maintaining quality of service (QoS);
- Optional Transient Fault Protection (TFP) that delivers parity checking on

all flops to address transient faults and provide additional permanent fault coverage to enable a significantly more efficient mechanism to achieve ASIL B in conjunction, with hybrid mode and the STL compared to the use of dual-core lock step;

- Memory protections on all caches; and
- AMBA interface protection on external interfaces.

FIG. 1
Cortex-A720AE



Premium Scalable, Efficient Performance

Targeted at the latest technology nodes and benefiting from micro-architectural improvements to deliver full system performance and power, Cortex-A720AE is designed to answer demands for more performance at greater power efficiency within the form factor and thermal constraints of electrical/electronic (E/E) architectures in the modern software-defined vehicle (SDV). This provides SoC designers with greater design flexibility to optimize the silicon area of the CPU cluster(s).

These levels of performance and efficiency are not just reserved for the premium vehicle market, as improvements are applicable across all product configurations. This means that the benefits can be leveraged for vehicle use-cases more constrained by cost and silicon area. Cortex-A720AE delivers

a 1.2x performance uplift over the Arm Cortex-A78AE, with a 10 percent improvement in power efficiency and equivalent area efficiency.[1] It also enables the latest Armv9.2A features for security, AI, and QoS. In addition, compatibility with DSU-120AE helps ensure Cortex-A720AE can be used in heterogeneous clusters with Cortex-A520AE to address multiple vehicle use cases that require increased power efficiency and a reduced silicon footprint.

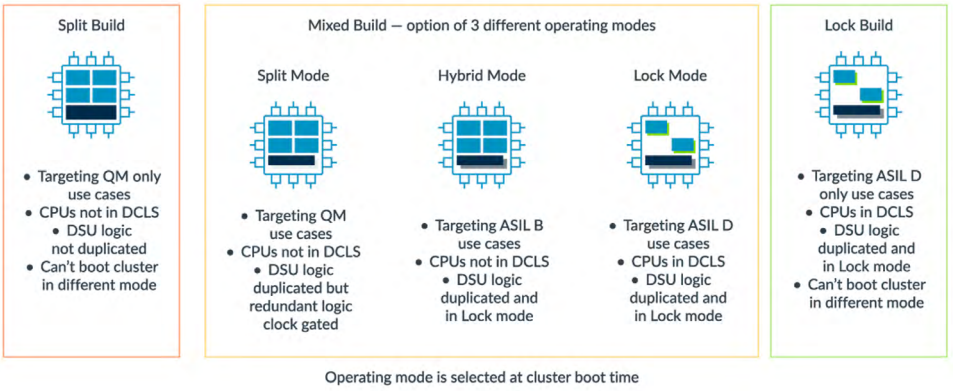
DSU-120AE is the latest AE Arm DynamIQ Shared Unit and brings a step-change in performance scalability for the CPU cluster. While the DSU-AE (the DSU for Cortex-A65AE and Cortex-A78AE) allowed up to four CPUs in a cluster with hybrid mode enabled, DSU-120AE increases this number to 14 to provide the SoC designer with improved flexibility. For example, where eight CPUs were required to meet performance targets, this would require two CPU clusters, each containing four CPUs, mandating the need for a coherent interconnect to connect the two clusters. Now this can be achieved through a single cluster of eight CPUs (or even lower due to CPU performance uplifts), saving power and silicon area and removing the need for a coherent interconnect if not required by other parts of the system.

This scalability has been enabled by significant micro-architectural enhancements. Highlights include:

- A new transport network scalable from a single node to dual-ring with options between one cache slice to eight cache slices to match;
- A massive increase in L3 cache hit bandwidth from 48GB/s for DSU-AE to 300GB/s for DSU-120AE; and
- Three new slice power-down modes to save on leakage power.

As well as performance scalability, DSU-120AE is key to delivering functional safety for the CPU cluster by enabling the split, hybrid, and lock operating modes, targeted at QM, ASIL B, and ASIL D use cases respectively.

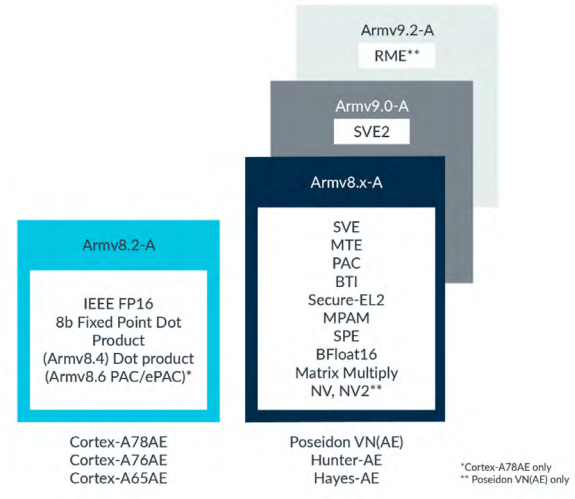
FIG. 2
Split-Lock: Flexible operations modes post-silicon



Bringing Armv9A to Automotive

Cortex-A720AE is built on the Armv9.2A architecture, with the introduction of Armv9-A bringing a significant uplift of architectural features to Arm Automotive Enhanced (AE) CPUs, including those that came in latter versions of Armv8-A. These features bring security, AI performance, and QoS benefits.

FIG. 3
Evolution of the Arm A-class Architecture



In terms of security enhancements, these include Pointer Authentication (PAC), Branch Target Identification (BTI) and Memory Tagging Extension (MTE). These features remove up to 95 percent of certain classes of vulnerabilities, including memory safety violations that account for the majority of all serious security bugs. MTE has proven to be hugely beneficial

to the Arm ecosystem because it allows developers to detect and avoid memory safety vulnerabilities before and after deployment. This helps speed up the application debugging and development process. Multiple Arm partners who are committed to tackling memory safety bugs in the software ecosystem have already built and enabled the MTE feature across their chipsets.

The new architectural features deliver a significant improvement in AI performance compared to the well-established Armv8.2A CPUs, with support for new data types introduced, such as BFloat16 and Matrix Multiply, as well as Scalable Vector Extensions (SVE2), the evolution of the Arm NEON SIMD engine.

FOOTNOTES

[1] Comparing Arm Cortex-A720AE and Cortex-A78AE implementation data in iso-configuration, iso-process, and at iso-frequency.

[2] Comparing Arm Cortex-A720AE and Cortex-A78AE SPECrate2006_int performance in iso-configuration, iso-process, and at iso-frequency.

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