CoreLink CMN-700: A Mesh for Modern Infrastructure

arm

Solution Brief

AT A GLANCE

To meet the rising demands of today's applications and customers, cloud service providers, carriers, system designers and others are increasingly turning to Arm Neoverse to build 5G networks, hyperscale data centers and high performance computing (HPC) systems. Arm Neoverse delivers leading performance and scalability while dramatically reducing power consumption and total cost of ownership.

WHY NEOVERSE CMN-700?

- Support for up to 256 cores per die/512 cores per system.
- Support for up to 512MB of System Level Cache (SLC).
- Enables high-bandwidth memory systems, with DDR5 and HBM2e/HMB3.
- Supports CCIX and CXL protocols for multichip and multi-socket connectivity.
- Supports the integration of PCIe Gen5 interfaces and 3rd party accelerators.

An Interconnect for the Next-Generation of Performant, Customized Infrastructure SoCs

Datacenter workloads and internet traffic are doubling every two to three years. At the same time, the requirements of cloud and wireless customers are becoming more complex and compute intensive with the emergence of specialized worklaod accelerators and real-time 5G services. To fulfill the promise of digital transformation, infrastructure providers must rethink their solution architectures to scale rapidly and economically.

Arm Neoverse CMN-700 is a high-performance, low-latency interconnect designed to meet the needs of tomorrow's infrastructure across a broad range of markets and use cases. Neoverse CMN-700 IP can be optimized for the following:

- Massive on-die core count, system level cache and mesh bandwidth scalability
- High bandwidth memory and IO systems with DDR5, HBM, and PCIe Gen5
- CCIX and CXL support for heterogeneous multi-die and multi-chip configurability

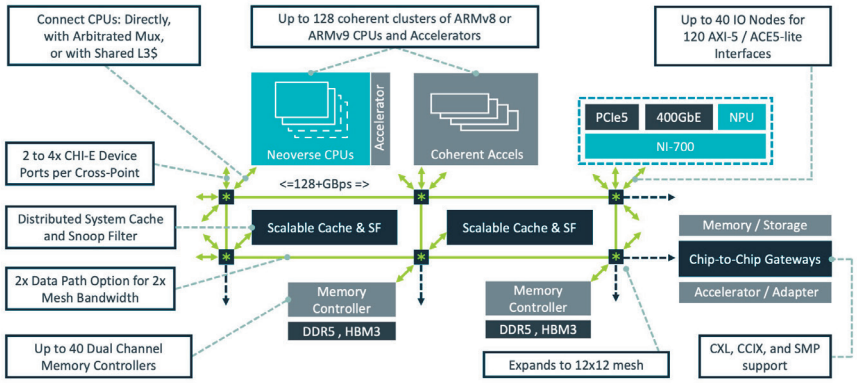
CMN-700 is our next-generation coherent mesh interconnect for linking processor cores, system level caches and accelerators within an SoCs to shared memory resources and I/O. CMN-700 enables high core count CPUs via chiplet and specialized processing via multi-chip SoCs. With CCIX and CXL support, CMN-700 supports traditional multi-socket systems or emerging use cases such as CXL-attached shared and pooled memory systems.

Creating a high-speed, high-performance, highly scalable fabric that can be readily adopted by semiconductor designers and equipment manufacturers additionally reduces design complexity and time to market. The end results are improved overall performance, reduced power consumption, fewer data bottlenecks, and reduced cost.

Platform Capabilities	CMN-600	CMN-700	Uplift
Number of direct CPU cores or DSU clusters per die / system	64 / 128	256 / 512	4x
Distributed System Level Cache (SLC) size per die	128MB	512MB	4x
Nodes (cross points) per die	64 (8x8)	144 (12x12)	2.25x
Devices per node (ex, CPUs, SLC)	2	3-5	2.5x
CHI / (AXI, CXS) Data path link widths	256b / (256b)	2x256b / (512b)	2x
# memory device ports (ex, DRAM, HBM) per die	16	40	2.5x
CCIX device ports per die	4	32	8x
CXL accelerator/memory attach support	No	Yes	New
MPAM memory and SLC monitoring & partitioning	No	Yes	New
Memory access protection with Memory Tagging Extension	No	Yes	New
CBusy and interconnect hot-spot re-routing support	No	Yes	New

CMN-700 vastly expands Arm's platform capabilities

Speed, Scalability, and Faster Time to Market



CMN-700 Block Diagram

A Coherent Mesh for Multiple Devices

CMN-700 is deployed as a high-speed mesh interconnect within an SoC, to link independent processors into a chiplet, to connect processor with main memory and I/O within a single system, and to link independent computer systems.

Accelerate Design Cycles

Socrates, a tool created by Arm, guides designers through the process of configuring and creating a viable interconnect, reducing the time and complexity typically required for implementing an interconnect mesh while simultaneously improving performance.

Coherent Multi Chip Links

CoreLink CMN-700's CCIX/CXL Gateways extend the high frequency, non-blocking AMBA 5 CHI protocol messages across multiple SoCs, so system designers can attach more compute or acceleration with a shared virtual memory.

Support for Open Standards

CMN-700 also supports AMBA AXI5, ACE5-lite, CXS, and CCIX. CCIX is the open coherency standard that allows processors based on different instruction set architectures to extend the benefits of cache coherent, peer processing to acceleration devices.

Agile Cache System

Keeping data on-chip greatly improves performance and efficiency. The integrated distributed system cache is designed to decrease average CPU read latency and boost IO throughput workloads, such as networking and storage.

For more information, please visit www.arm.com/products/silicon-ip-system/corelink-interconnect/cmn-700